



中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

ATLAS实验上的 硅径迹探测器升级

徐子骏

2022年7月15日

个人简介



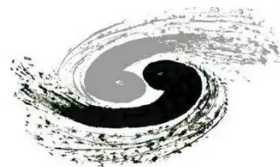
2007-2017, 北京大学, 学士 & 博士



2013-2017, 美国Fermilab, 访问学者



2017- 2022, 美国SLAC/斯坦福, 博士后

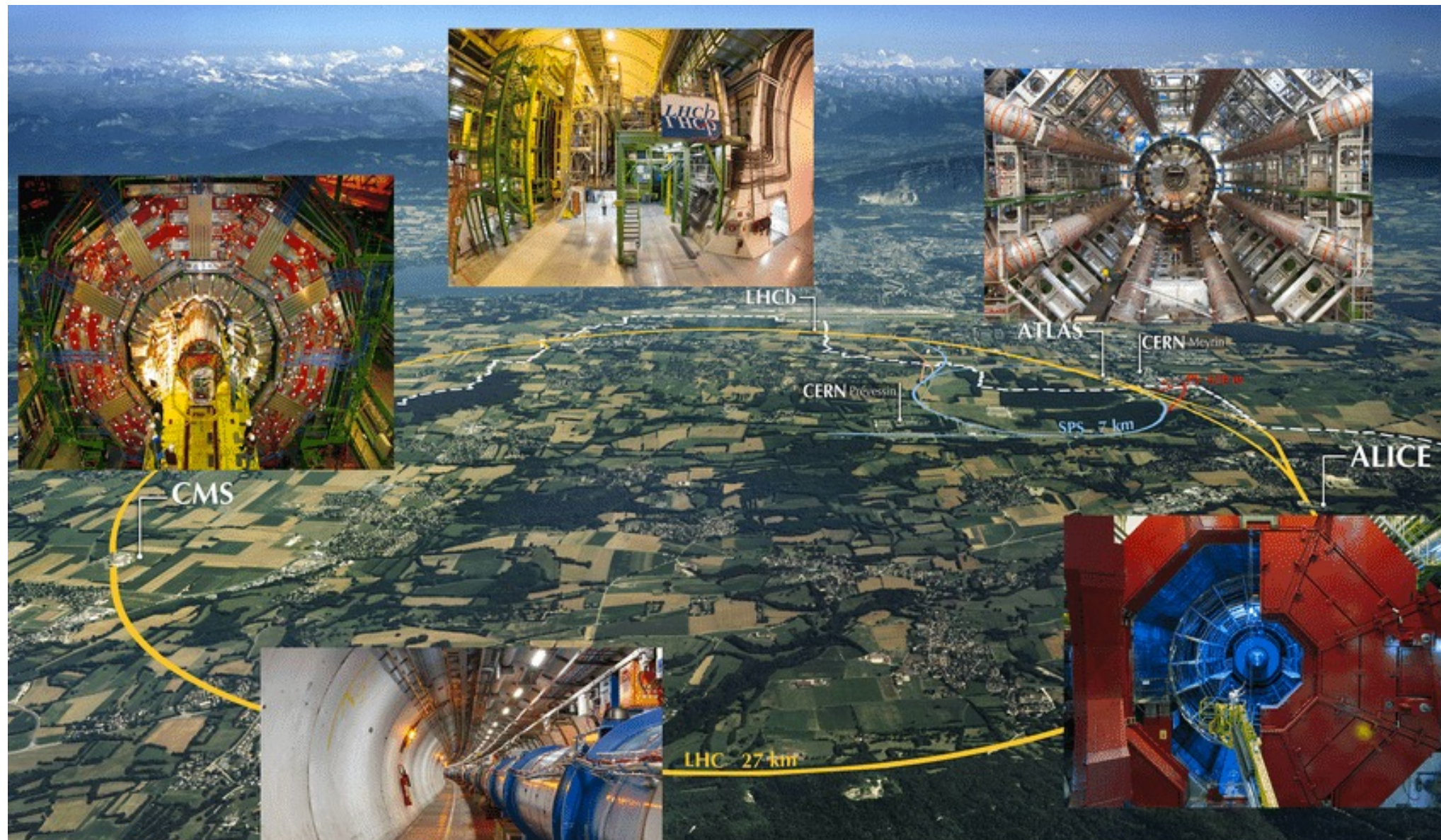


2022-现在, 中科院高能物理研究所, 研究员

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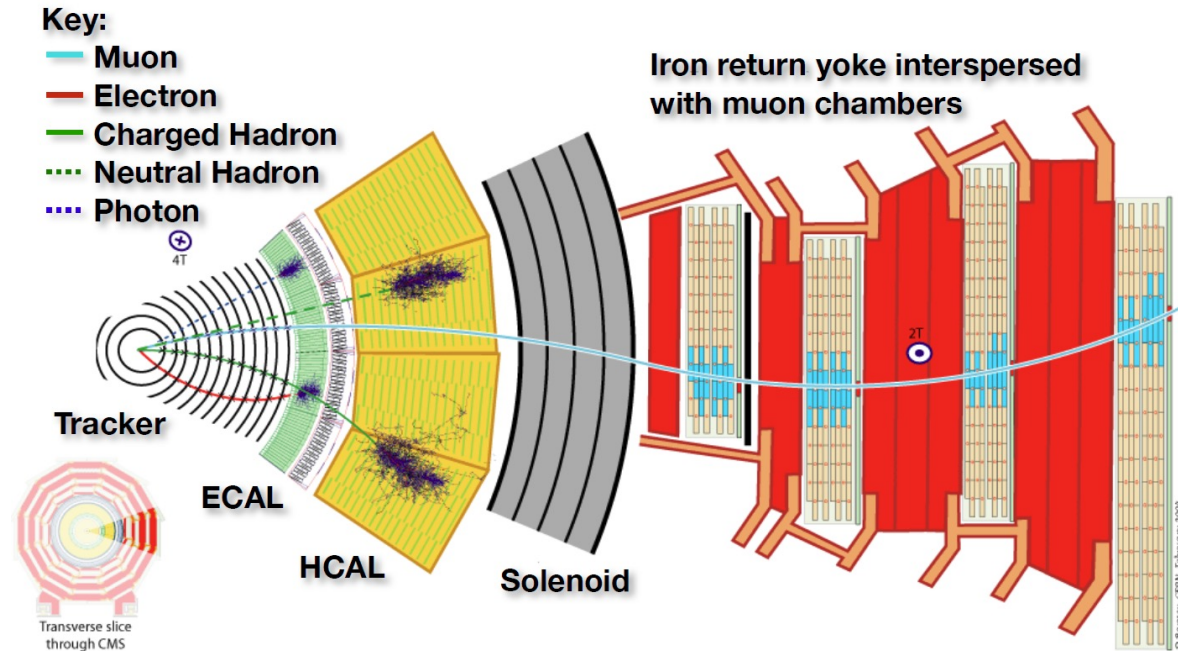
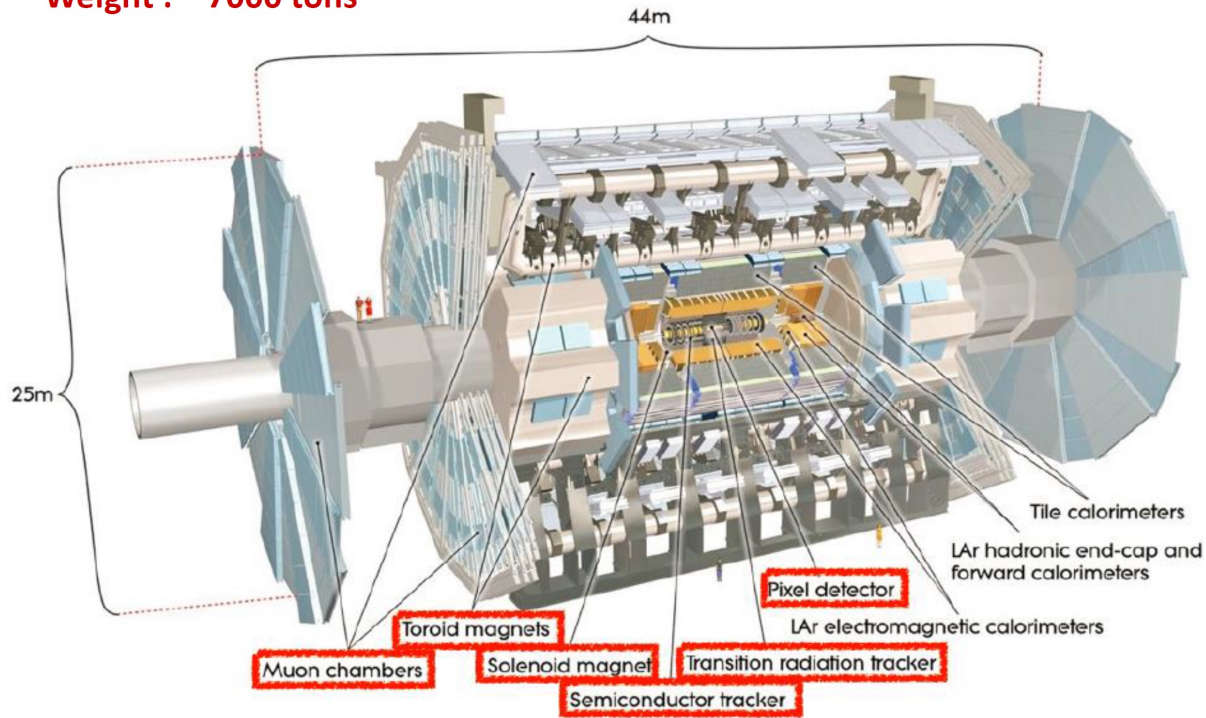


大型强子对撞机LHC：2012年ATLAS&CMS发现Higgs粒子



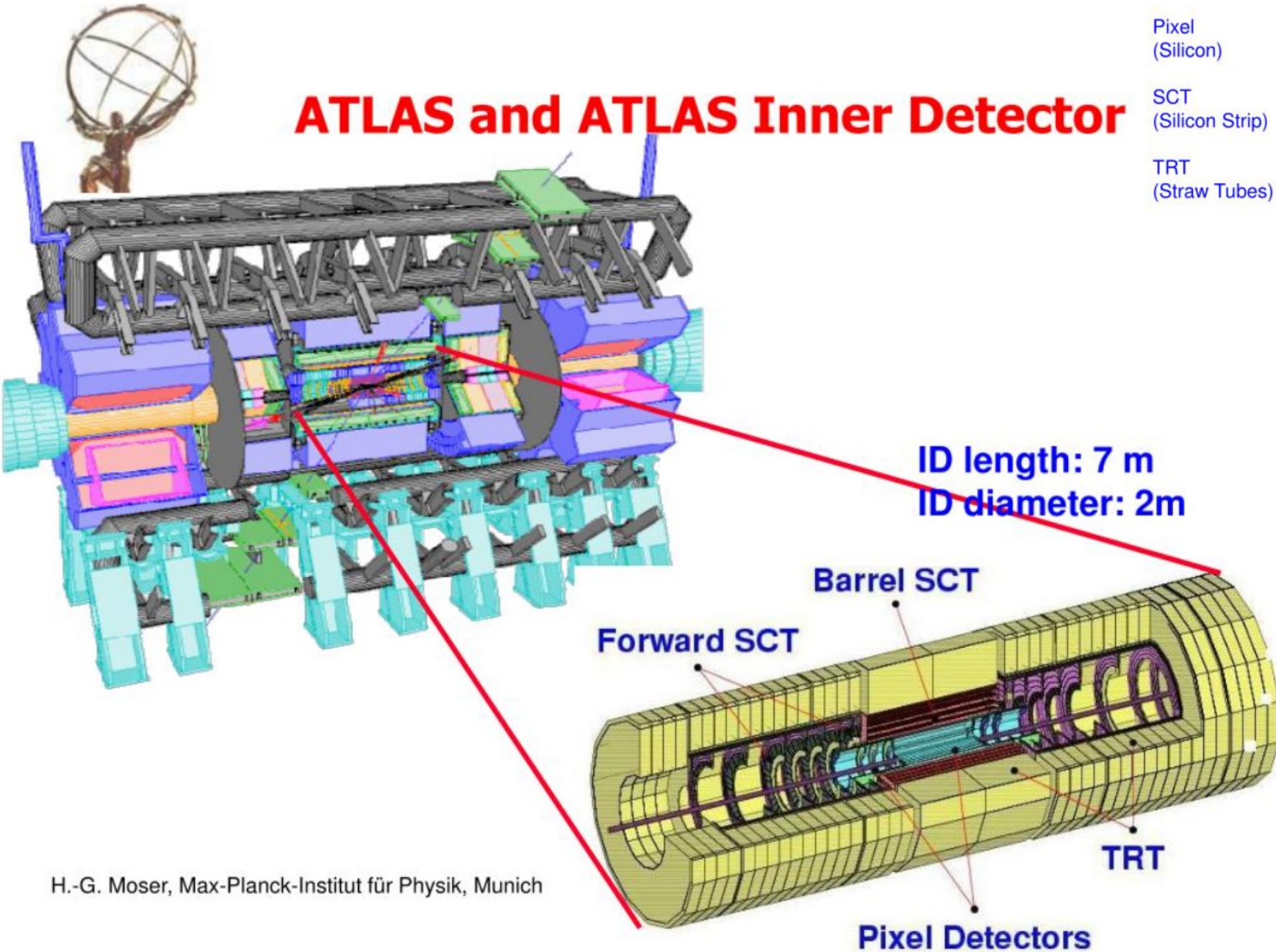
ATLAS 与 CMS 探测器

Weight : ~ 7000 tons



ATLAS and ATLAS Inner Detector

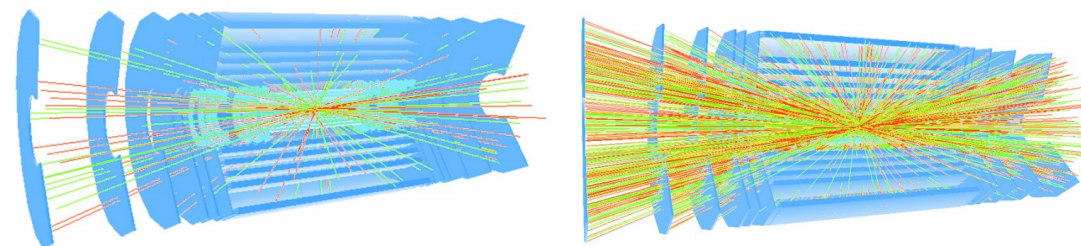
Sub-Detector	r(cm)	element size	resolution	hits/track	channels
Pixel (Silicon)	5-12.5	50 μ m x 400 μ m (3D)	12 μ m x 60 μ m	3	93x10 ⁶
SCT (Silicon Strip)	30-52	80 μ m x 12cm (stereo)	16 μ m x 580 μ m	4	6x10 ⁶
TRT (Straw Tubes)	56-107	4 mm x 74cm (projective)	170 μ m	36	0.4x10 ⁶



H.-G. Moser, Max-Planck-Institut für Physik, Munich

高亮度-大型强子对撞机 (HL-LHC)

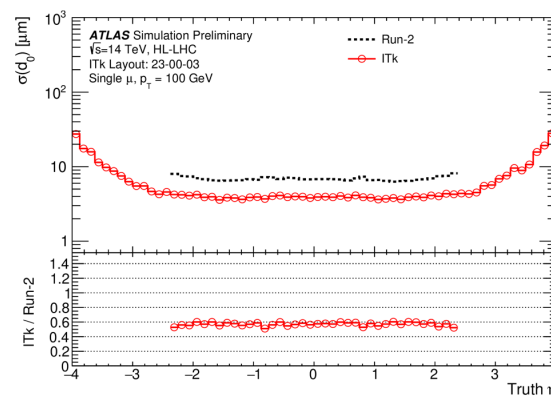
- 2025~2027年，LHC升级为HL-LHC
 - 平均collisions/BC: $\sim 30 \rightarrow \sim 200$
 - 峰值亮度: $1e34 \rightarrow 5-7e34 \text{ cm}^{-2}\text{s}^{-1}$
 - 积分亮度: $350 \rightarrow 4000 \text{ fb}^{-1}$
 - 10倍数据量：精确测量、新粒子、新物理



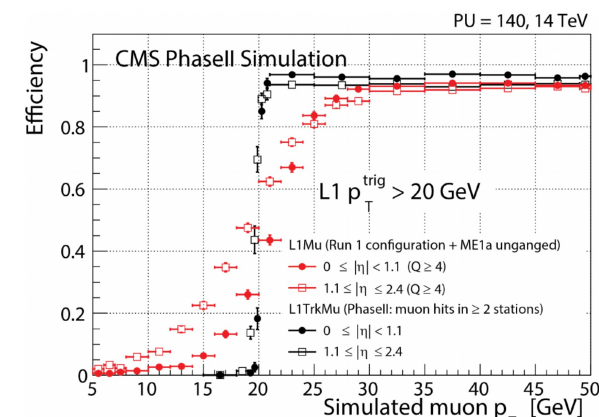
23 pile-up \rightarrow 230 pile-up [1]

- LHC上的探测器

- 提高抗辐射能力
- 提高时空间测量精度，减少本底
- 升级配套的触发和读出系统



ATLAS ITk



CMS L1-Trk

ATLAS二期ITk径迹探测器

- 全硅径迹探测器 (ITk) 替代现有径迹探测器 (ID)

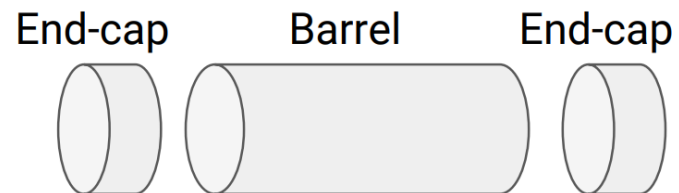
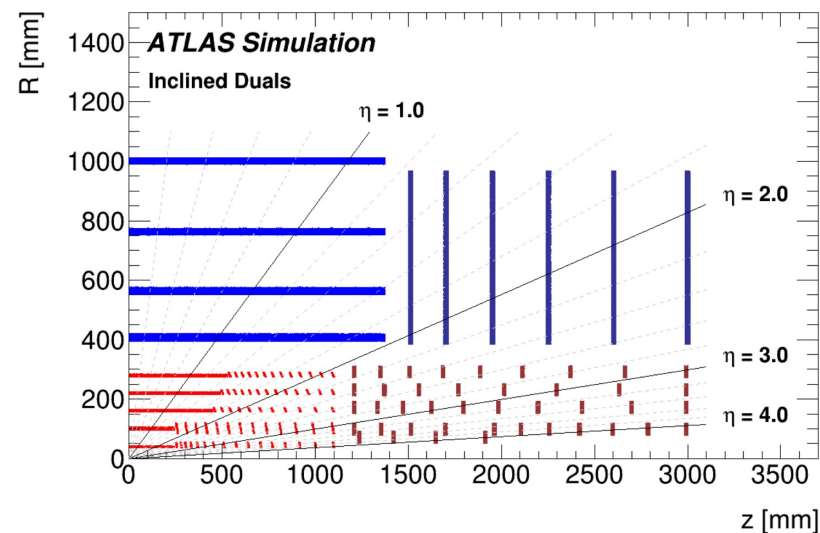
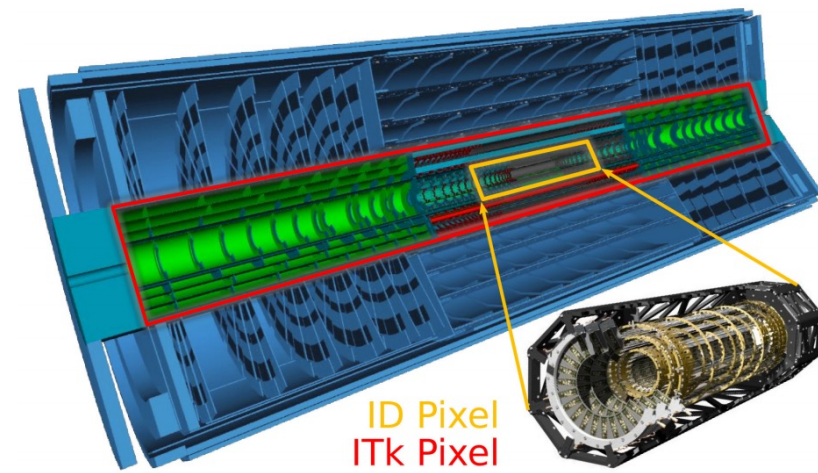
- 硅像素探测器总覆盖面积: $1.7\text{m}^2 \rightarrow 13\text{m}^2$ ($5\text{e}9$ 测量道)
- 原始数据读出速度提高 $O(100)$ 倍
- 领域内最前沿的硅探测器和电子学技术
- 直接影响ATLAS上几乎所有的物理研究：**不能失败！**

- 最内两层硅像素探测器由美国ATLAS合作组负责

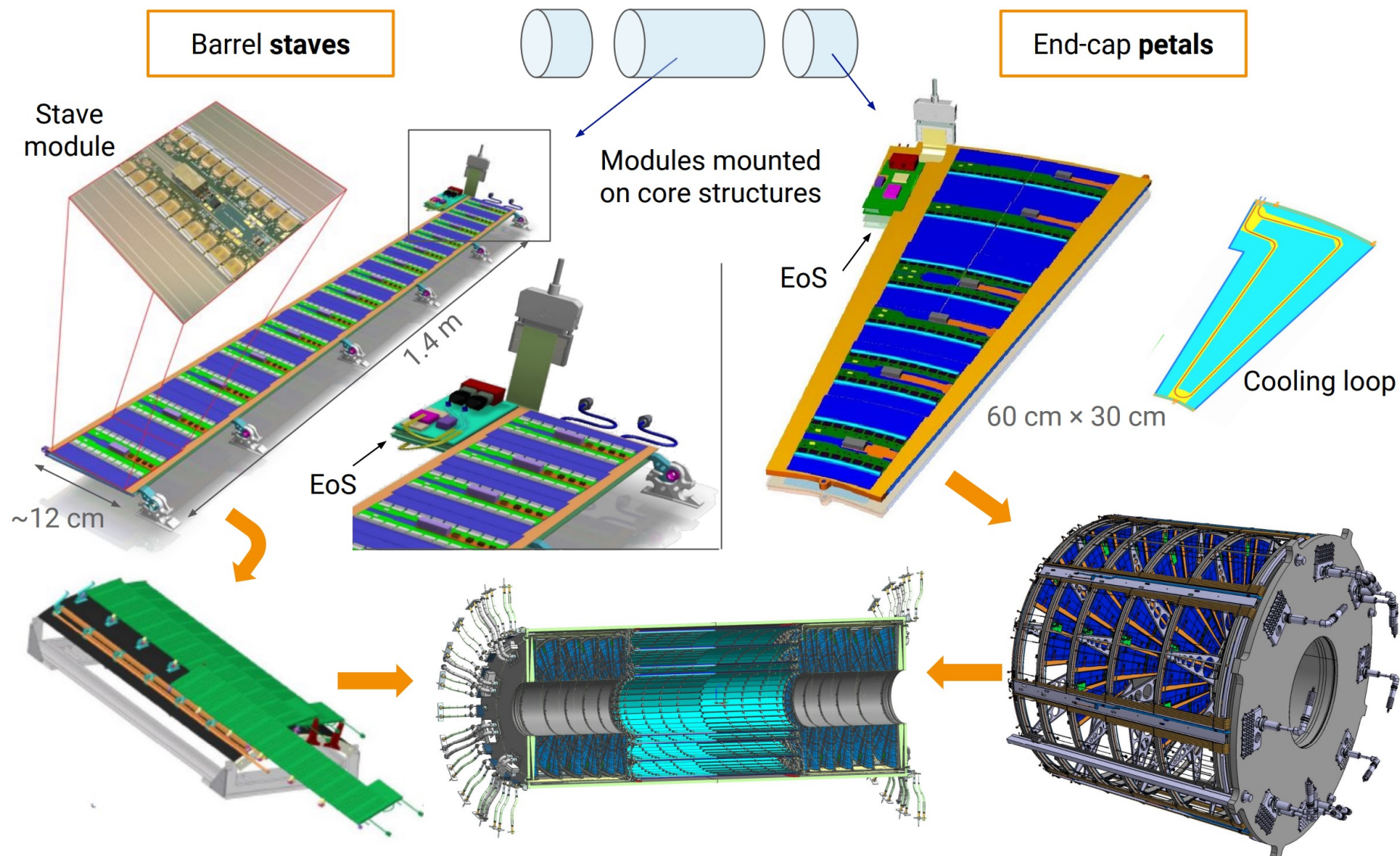
- 体积小，工程难度大
- 插入式可替换设计，HL-LHC一半寿命

- 外层硅微条探测器

- 中科院高能所与清华大学合作：硅覆盖面积约10平方米，约占桶部总面积10%，为国内首次承担此类大面积抗辐照硅径迹探测器项目

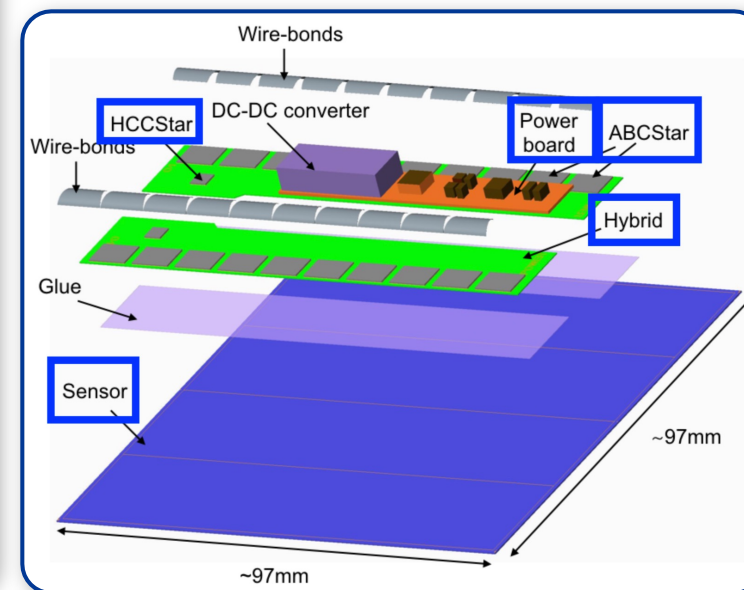
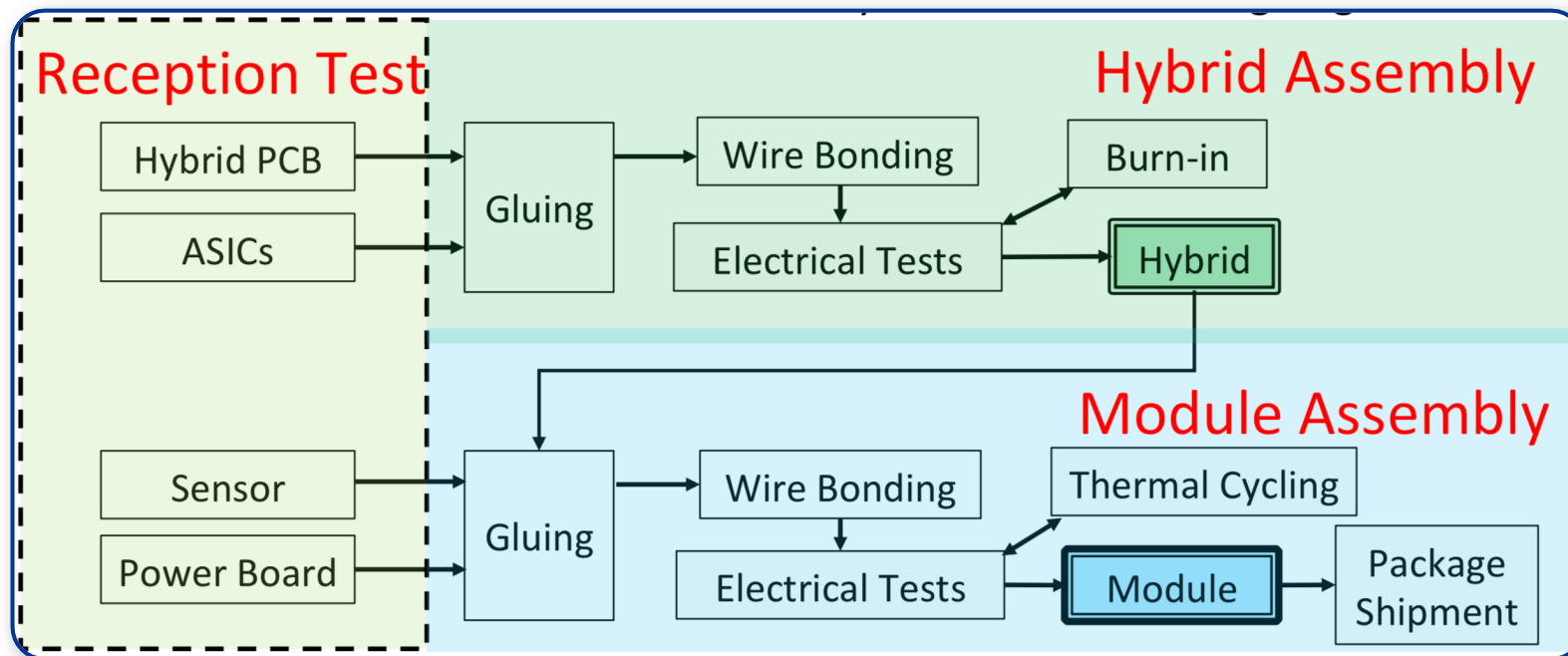
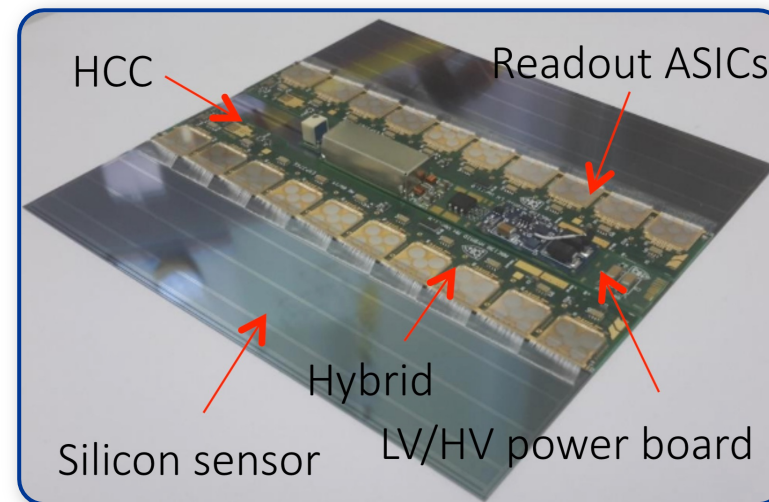


探测器结构：桶、端盖



硅微条模块建造流程

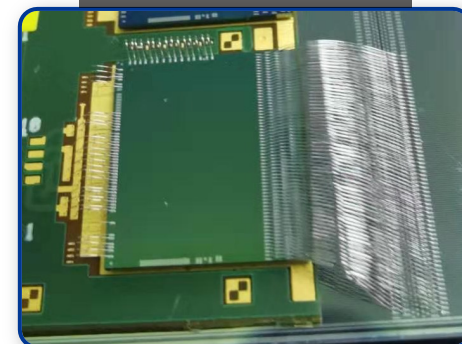
- 持续推动建设国内实验室，开展预生产工作
- 关键技术如高速线邦定和高低温测试



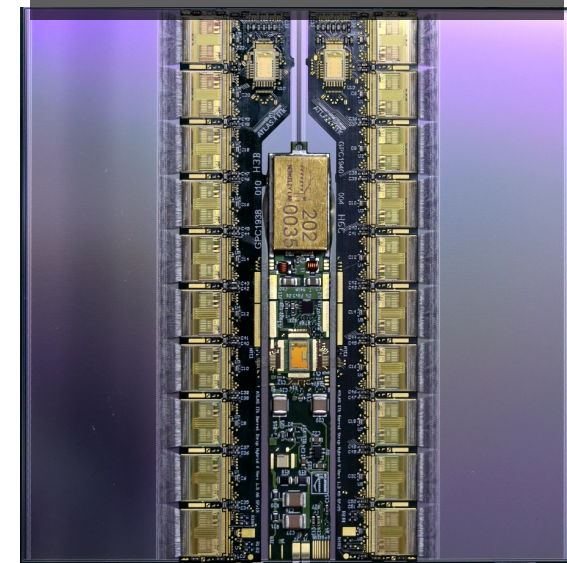
硅微条模块建造

- 承担研制1000个桶部硅微条探测器模块（硅传感器表面约10平方米，占总共的10%）
- 已掌握高速线邦定、自动精准点胶、高精度非接触测量等关键技术
- 正在逐步完成（~80%）模块站点审核、读出芯片与传感器的抗辐照研究

高速线邦定

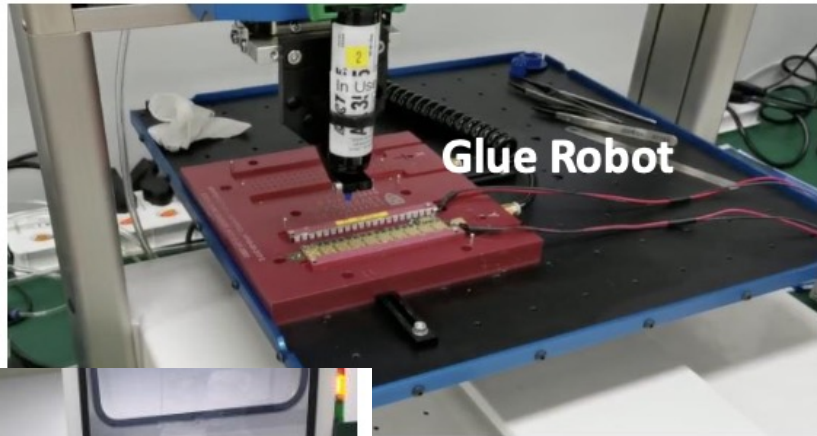


短微条模块 (5120道)

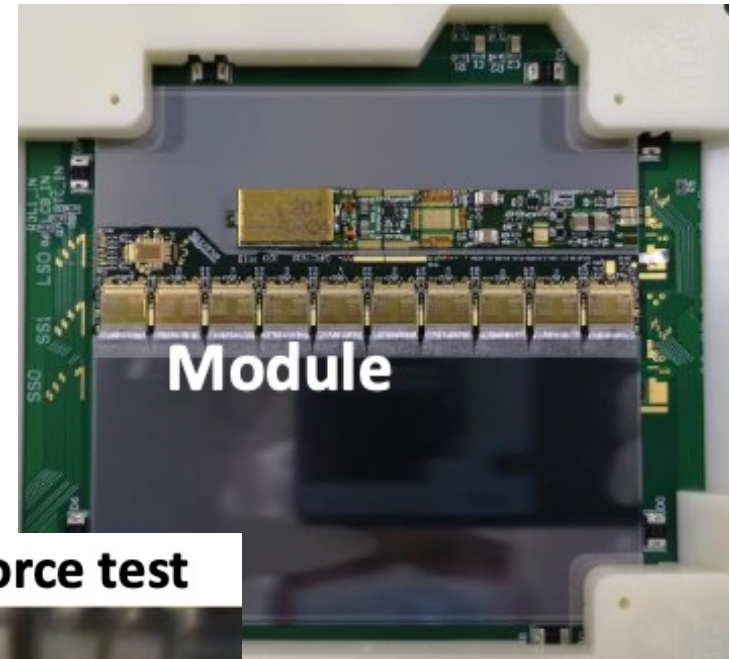
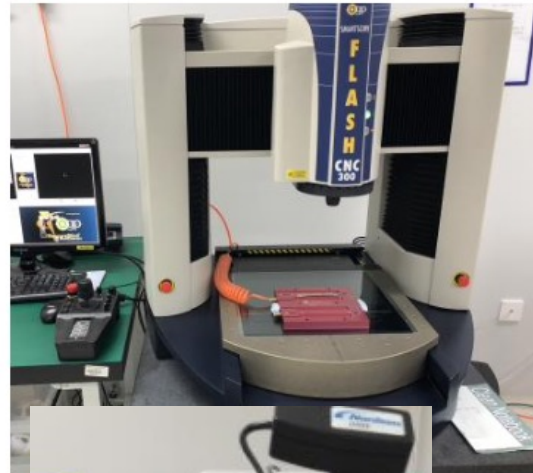


硅微条模块建造

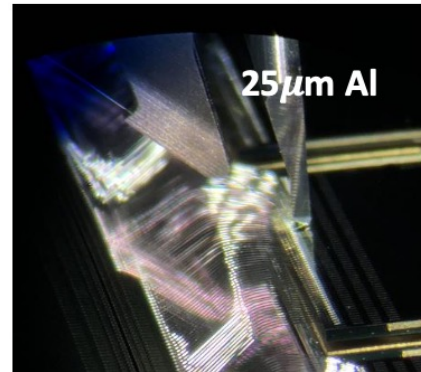
Calibration of glue amount



Metrology of glue thickness



Wire bonding



Pull tester

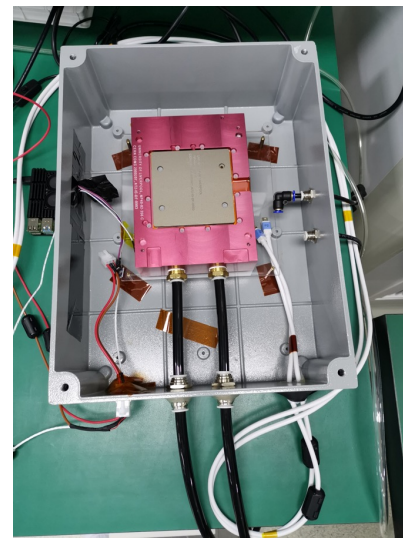
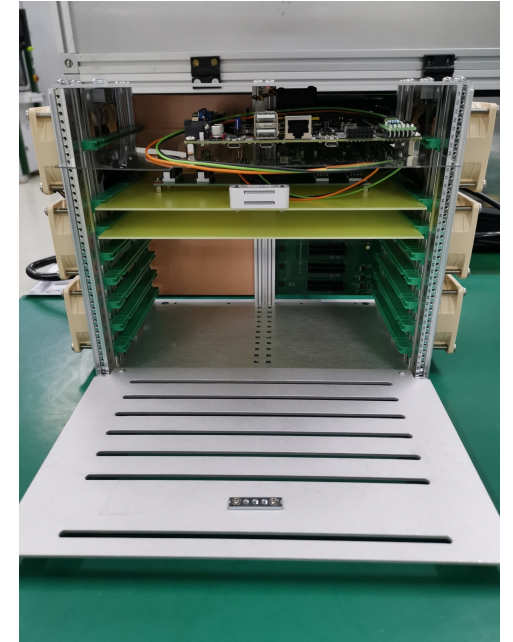
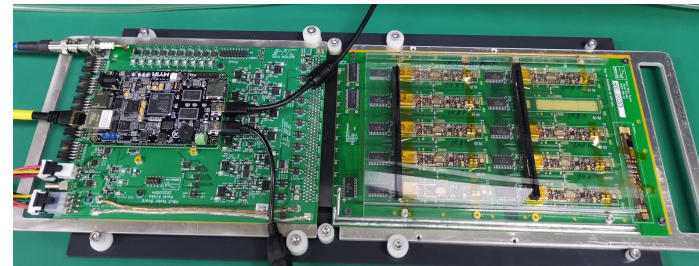
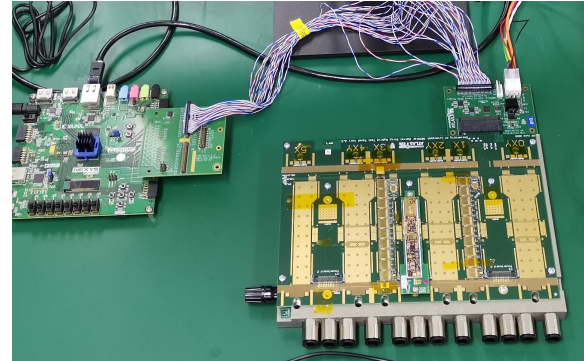


Pull force test



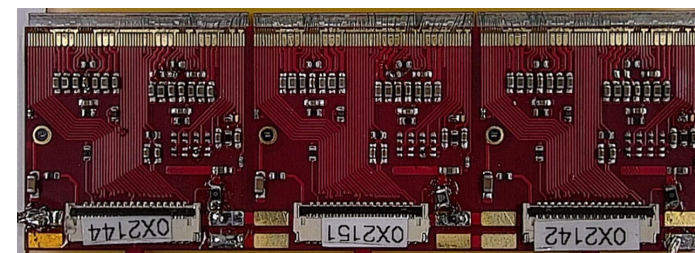
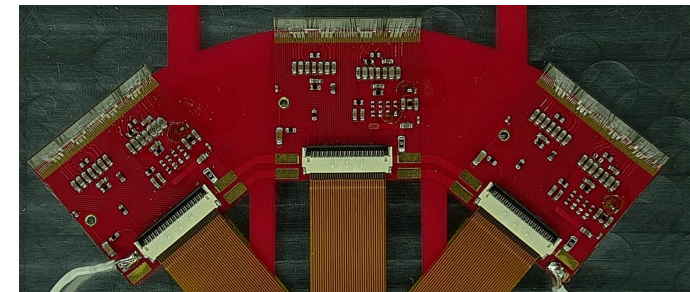
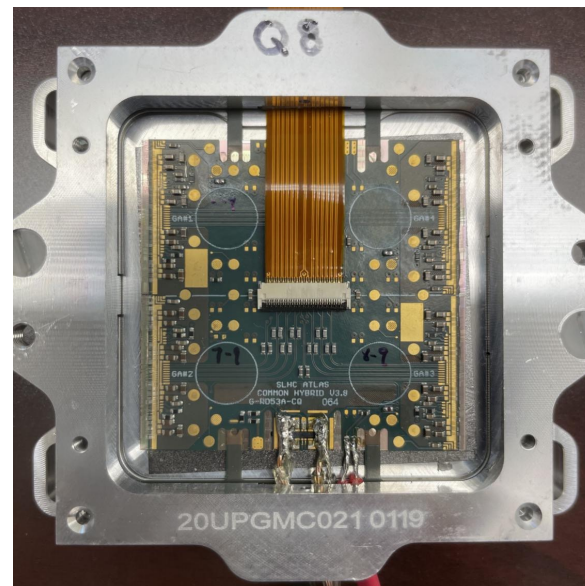
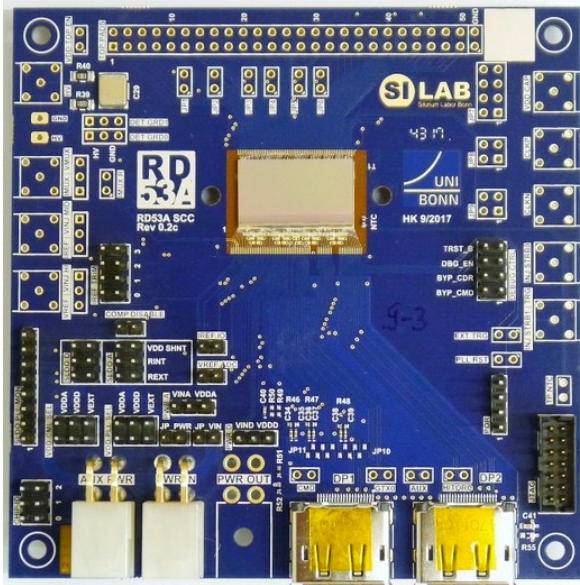
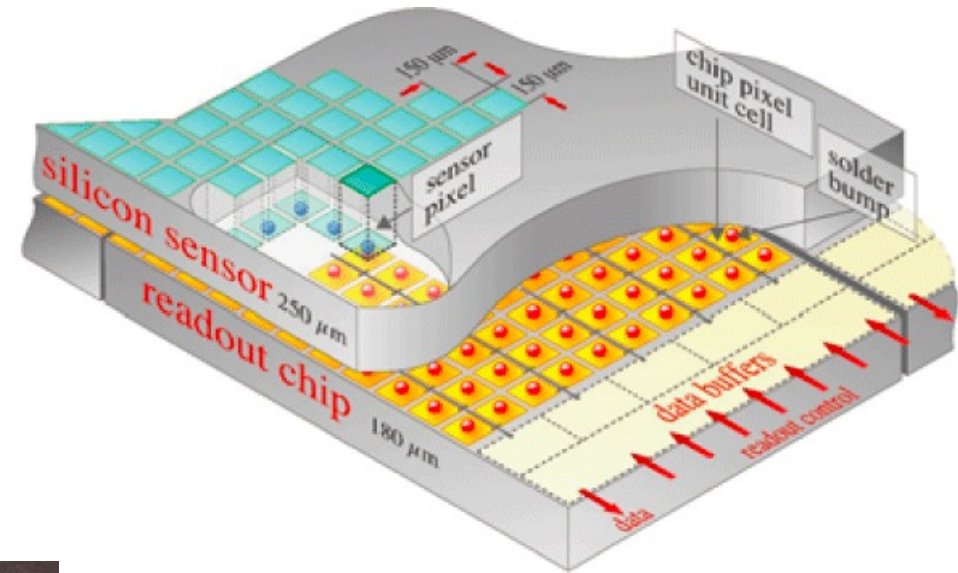
测试，老化，冷热循环

- 为确保探测器模块长期稳定运行，还需要对模块上的关键部件如绑定完的控制PCB板进行老练测试。
- 环境箱温度设定在 40°C ，控制PCB加电运行约100个小时
- 冷热箱内完成10个 -35°C 至 $+40^{\circ}\text{C}$ 热冷循环测试
- 包含低温启动测试及最后的加载高压运行测试，整个过程预计持续12个小时，以模拟未来探测器运行环境

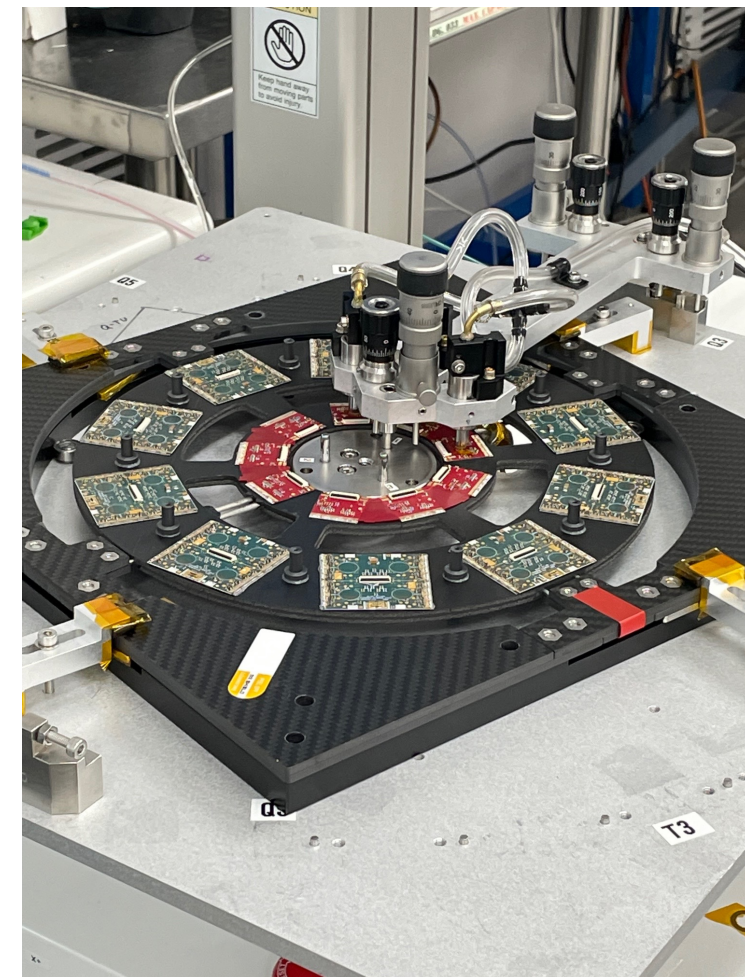
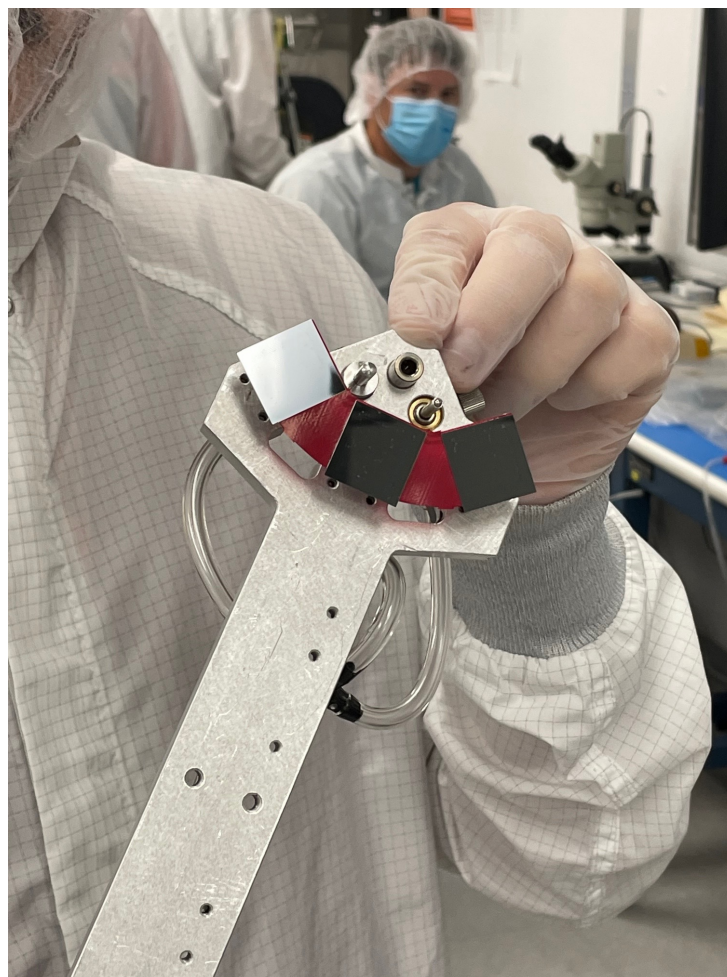
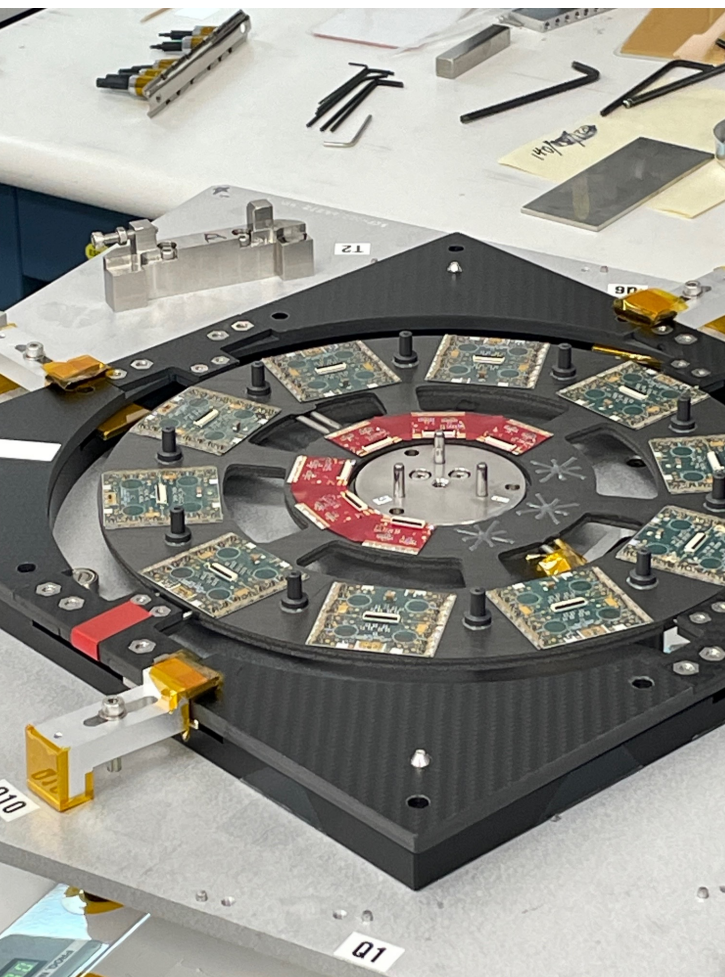
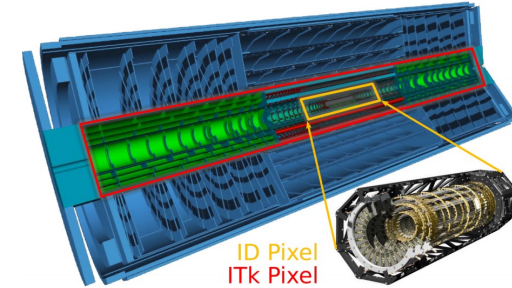


硅像素前端芯片Rd53：ATLAS与CMS联合设计

- 硅像素探测器前端芯片需要全新设计：Rd53
 - 65纳米CMOS工艺
 - 像素尺寸 $50 \times 50 \mu\text{m}^2$ 或 $25 \times 100 \mu\text{m}^2$
 - Rd53a用于原型开发，Rd53b用于最终量产
 - ITkPixVx 是在ATLAS上使用的Rd53b芯片



ATLAS ITk探测器组装



前端芯片Rd53

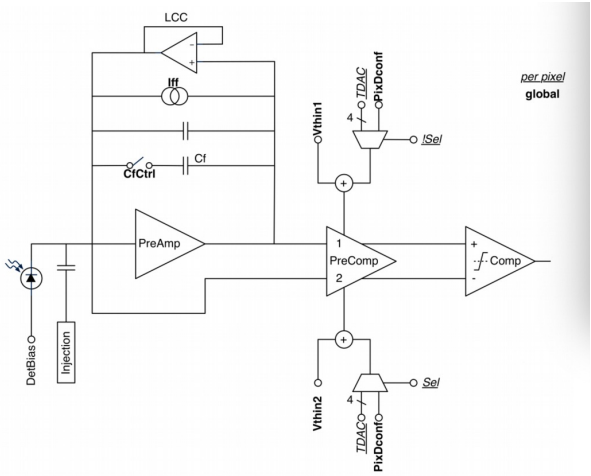


Figure 17: Schematic of Differential front end flavor.

- Rd53的输入和输出决定了数据传输系统的设计
 - 单路Cmd输入，160 Mb/s
 - 无需额外输入时钟信号：简化探测器设计
 - CDR模块从输入流中提取时钟信号，用于整个芯片的运行
 - 四路data输出，每路1.28Gb/s

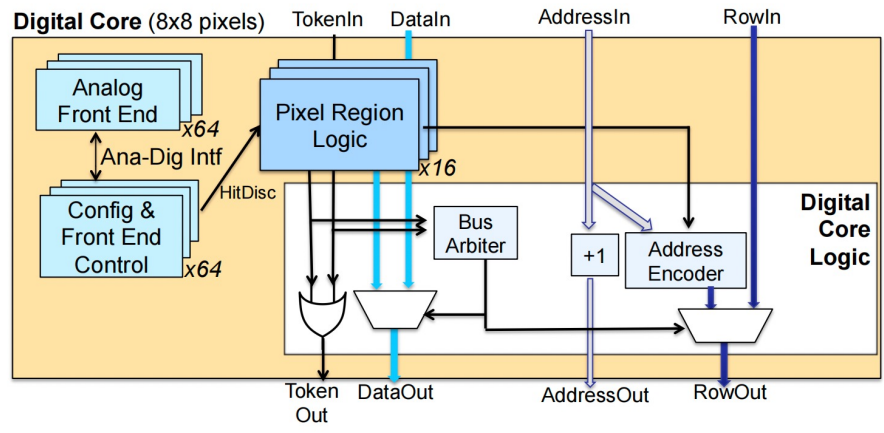
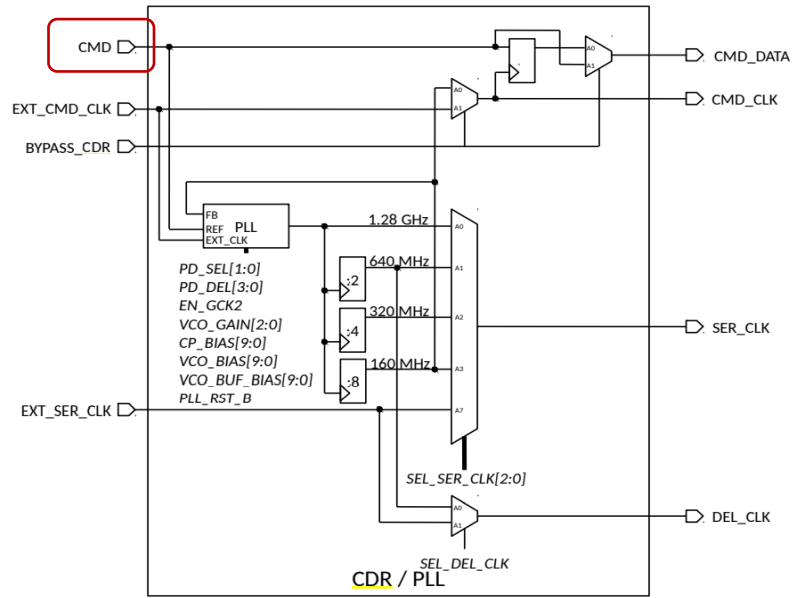


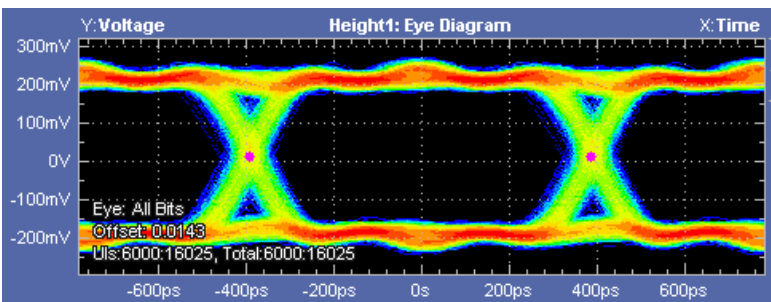
Figure 31: Block diagram of digital core with multiple regions.



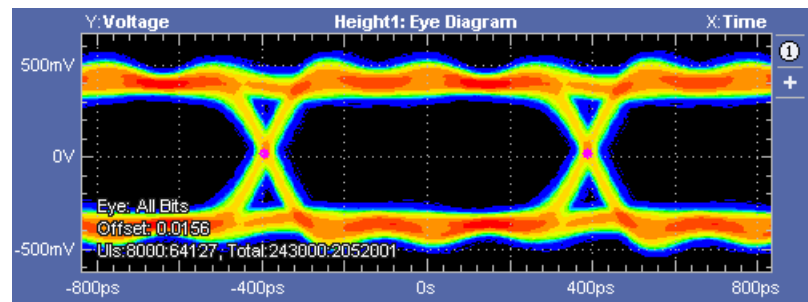
Rd53的输入和输出

- Bonn大学团队重新设计了CDR电路，并单独生产了测试芯片 -> 输出时钟稳定
- Rd53a芯片外挂CDR测试芯片，可等效实现Rd53b芯片的数据传输性能
 - **提前1年预知了Rd53b的性能** -> ITk数据传输系统设计和测试不依赖于Rd53b芯片（高风险、易延期）

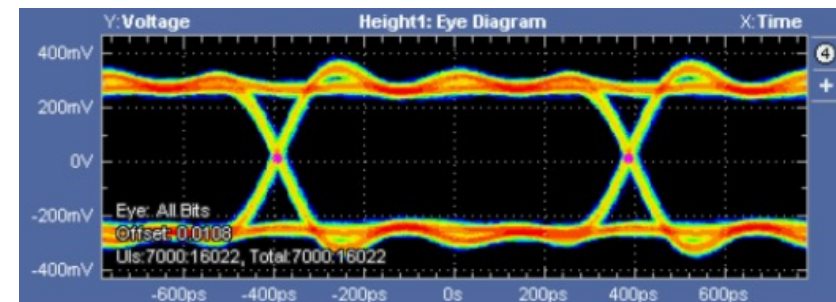
Rd53a



Rd53a+ new cdr

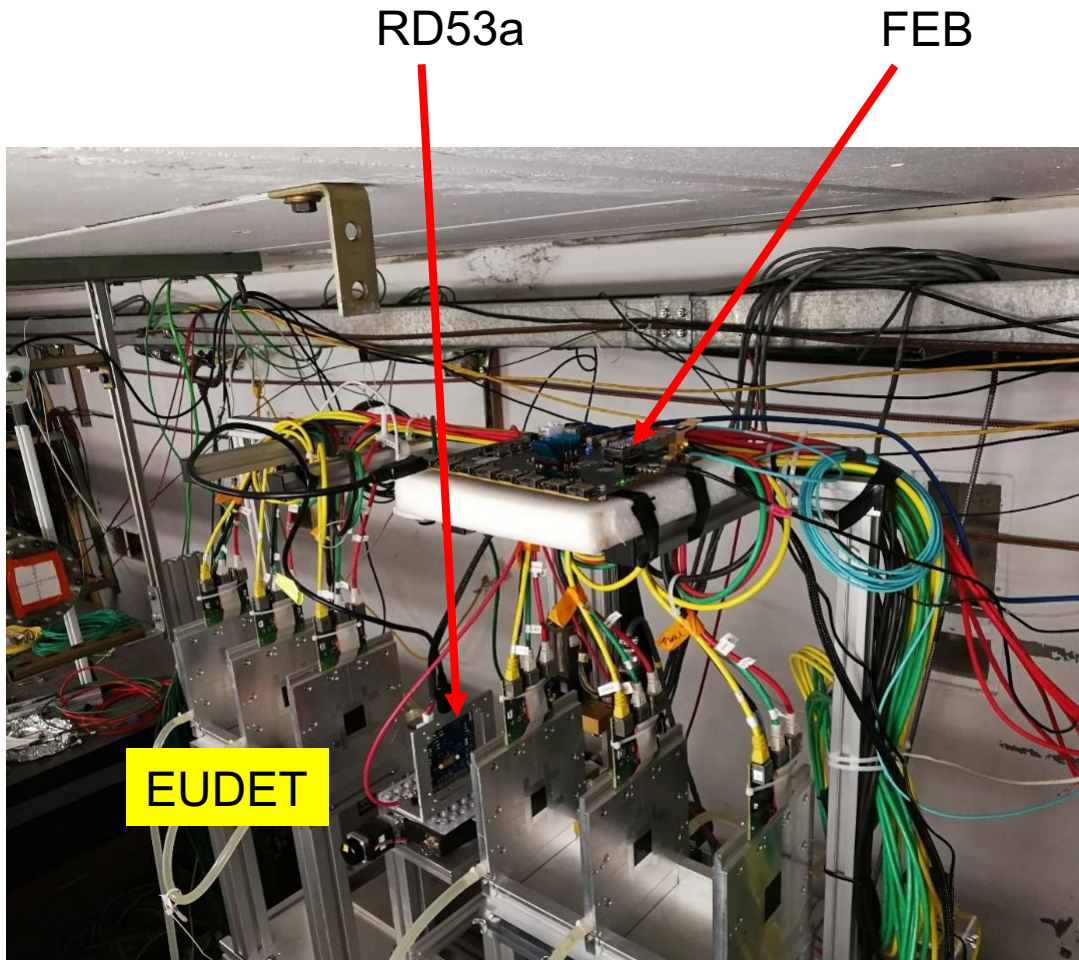


Rd53b (ITkPixV1)



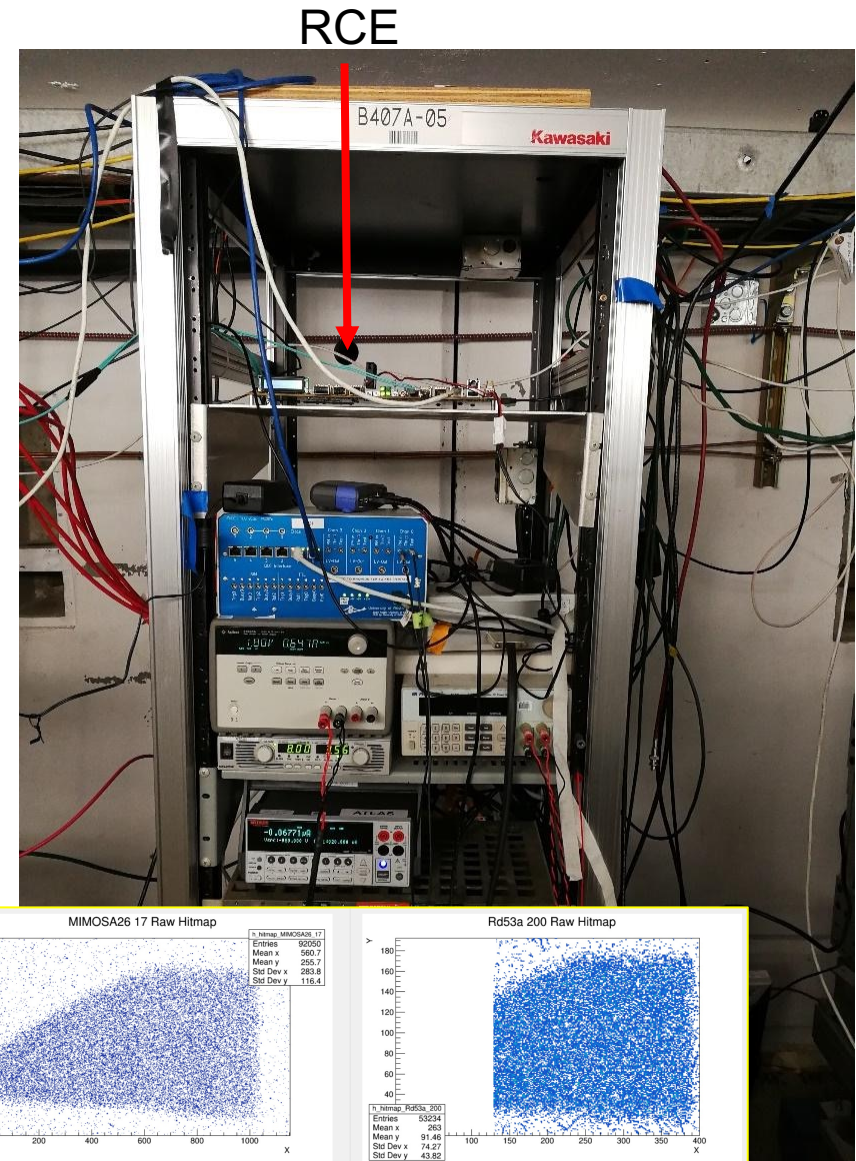
Rd53b (ITkPixV1) 性能略好于“等效Rd53b”，均远好于Rd53a

RD53a 束流测试, 2019

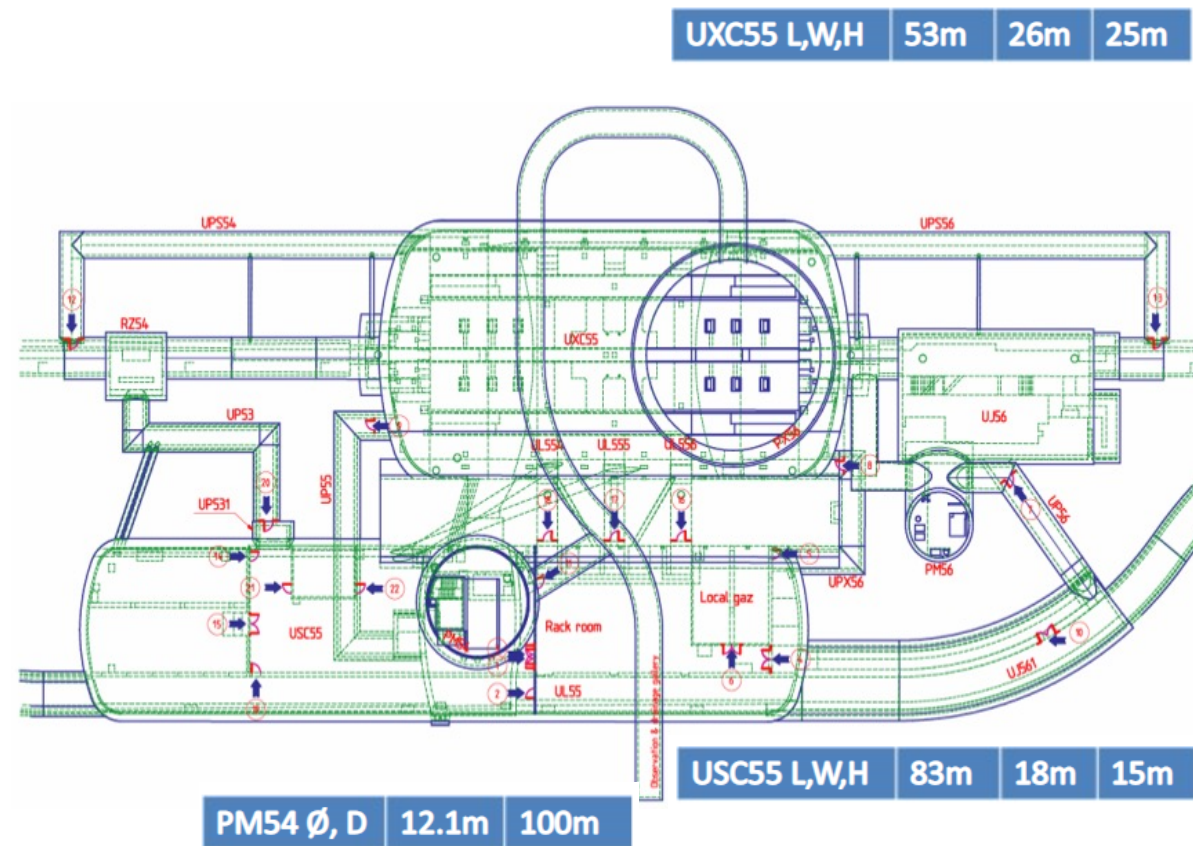
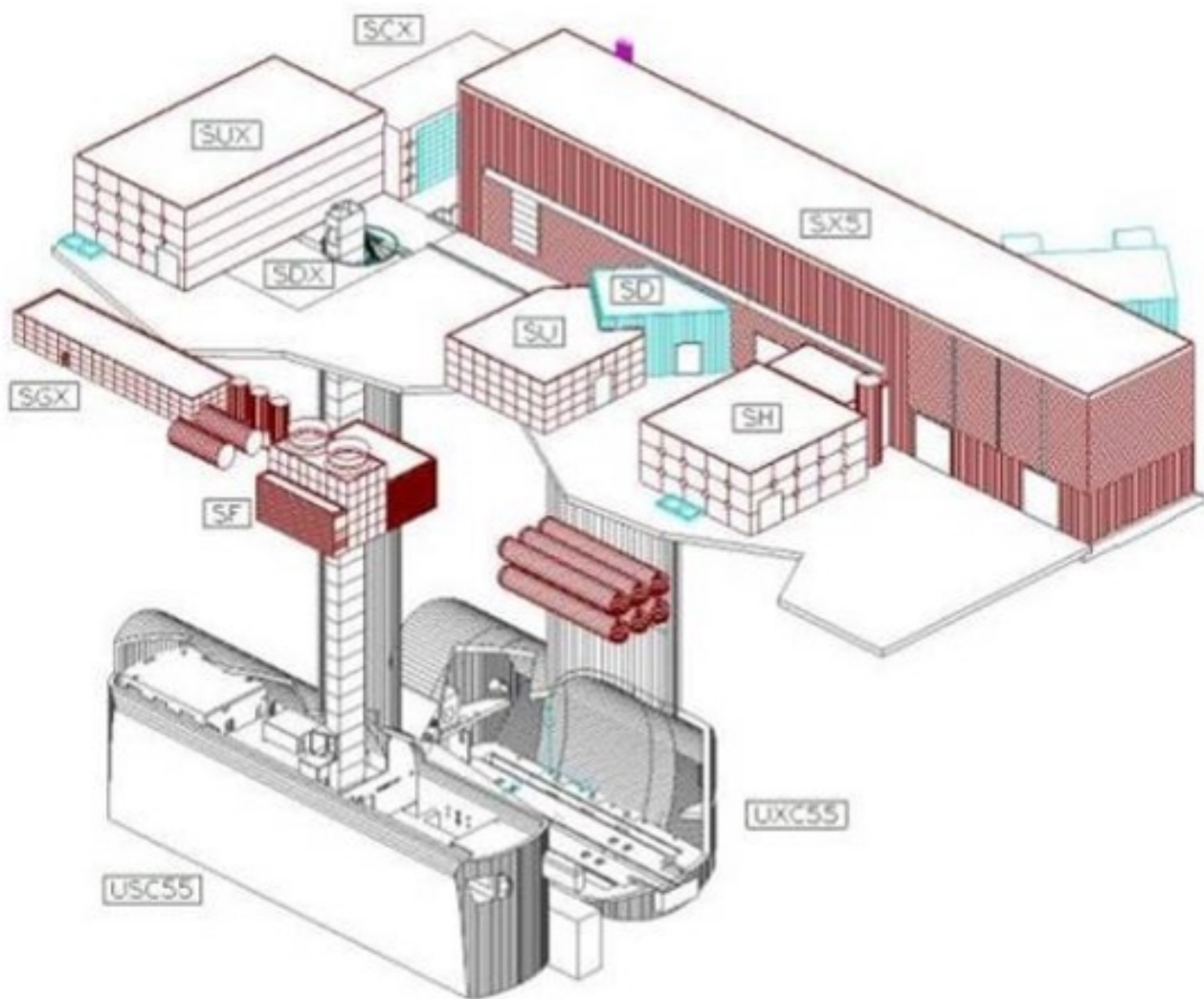


<https://confluence.slac.stanford.edu/pages/viewpage.action?pageId=24229540>

9



CMS实验区 (ATLAS类似)



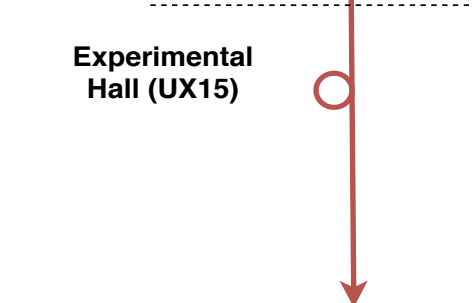
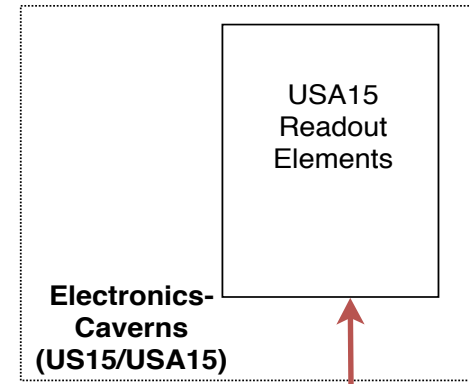
ITk的数据传输系统：探测器模块 ↔ DAQ

- 双向数据传输系统

- DAQ发送指令到探测器模块；探测器模块将数据传送到DAQ

- Optobox为前端探测器和后端读出系统之间的枢纽（电 ↔ 光）

- IpGBT芯片为CERN主导开发，用于辐射环境下的高速数据传输
 - 通用设计，配置丰富，用法灵活，可广泛用于不同的实验
- 使用无源电路连接前端探测器模块
- 通过商用光纤接到后端读出系统

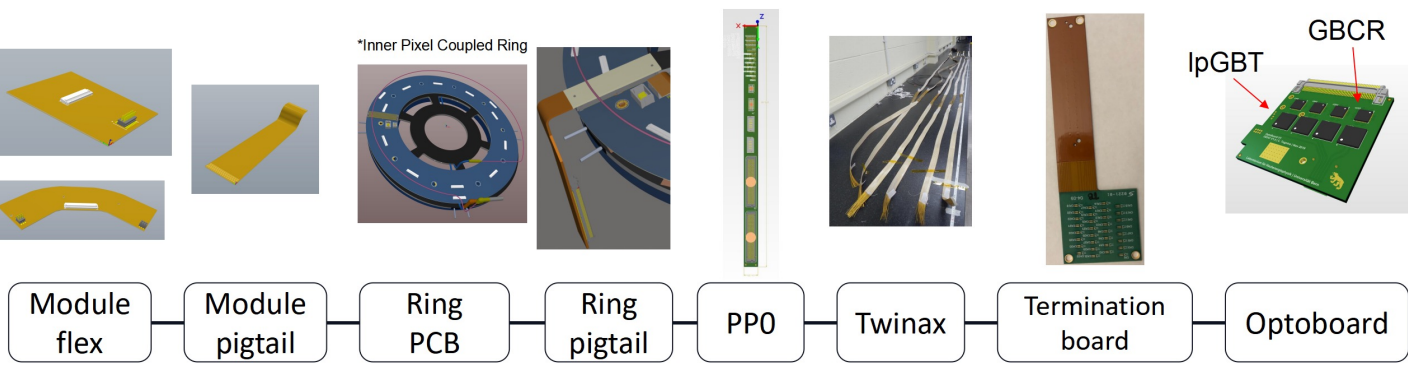
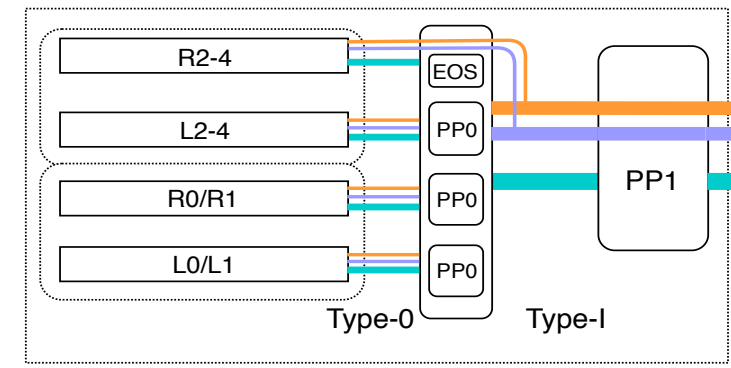


Optobox

Data

Clk/Cmd

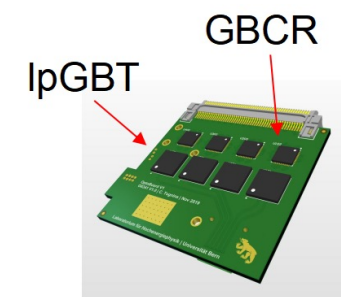
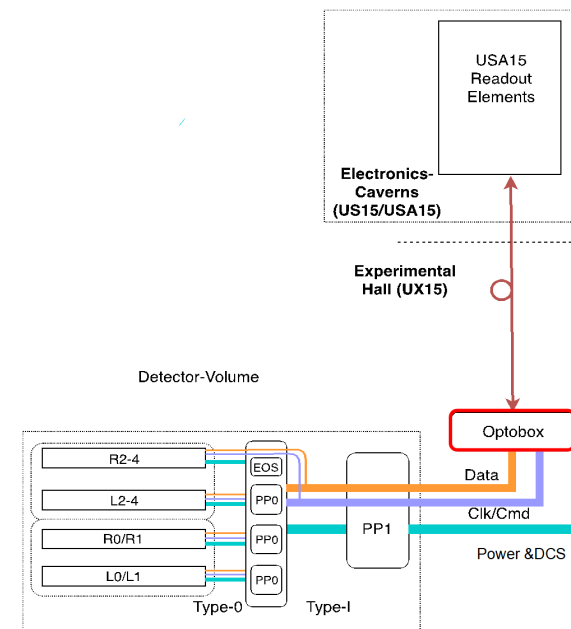
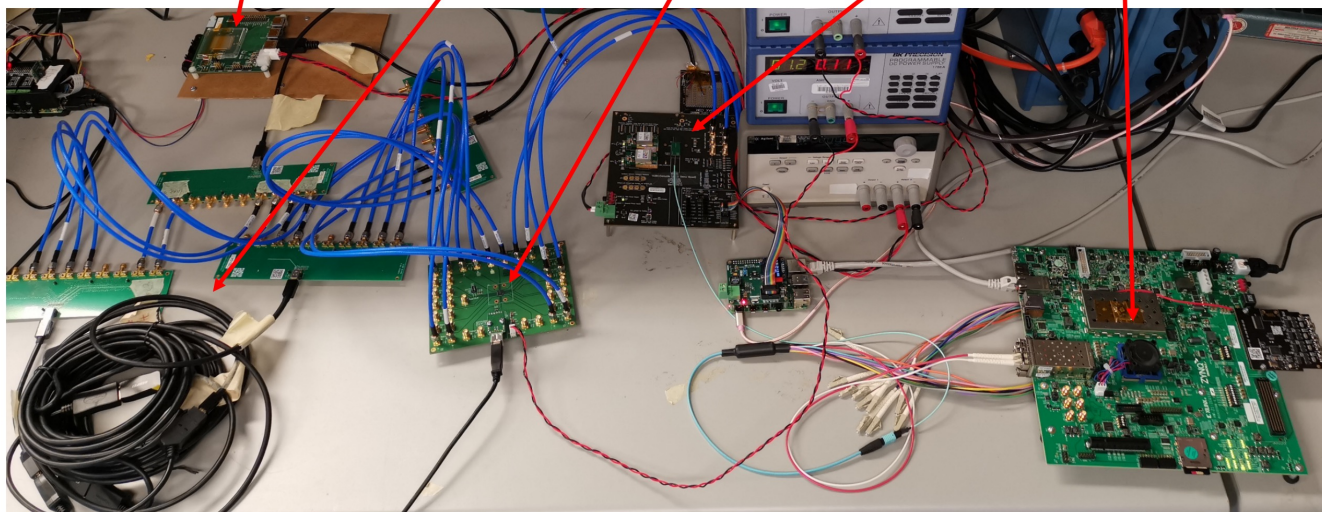
Detector-Volume



SLAC设计、测试

2021年夏，全链测试

ITkPixV1 + cables + GBCRv2 + IpGBTv0 + DAQ

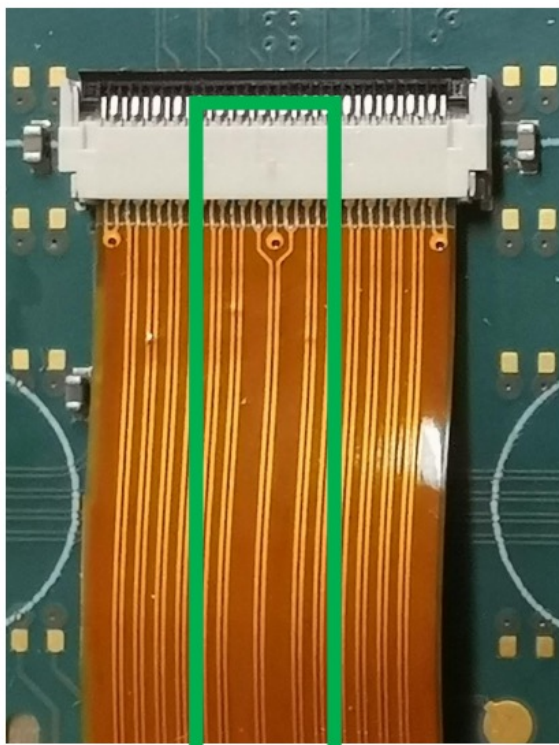


- **实现全链系统稳定运行**：探测器模块 ↔ 无源电导线 ↔ “optoboard” ↔ 光纤 ↔ RCE DAQ
- 最终系统中的所有（“等效”）组件全部被测试
- 难点：1）每个芯片都需要配套的控制系統；2）所有组件同时正确的运行
- 此平台为各个组件后续的开发、升级和测试提供了坚实的基础，譬如
 - RCE DAQ 可换成 FELIX DAQ
 - 新版optoboard

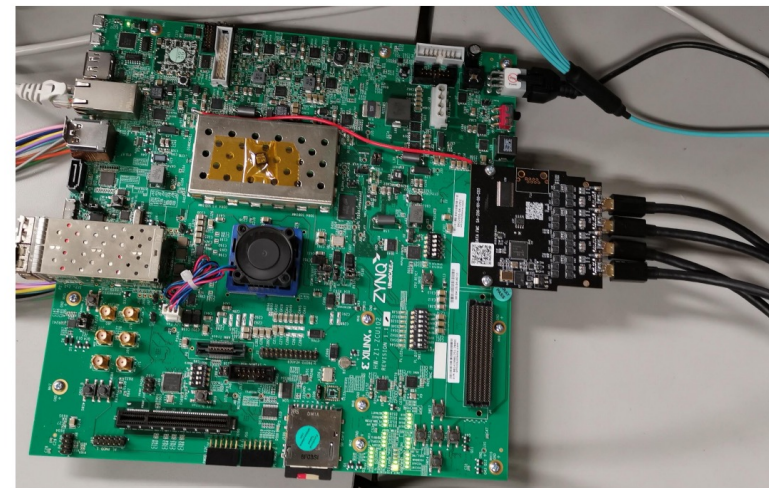
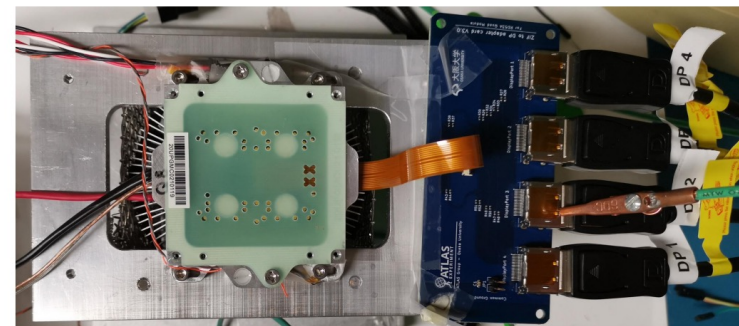
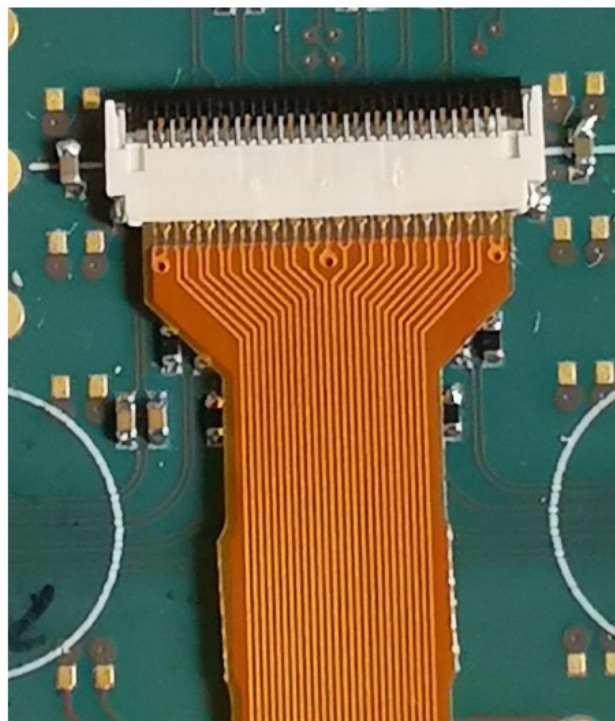
Rd53a 模块的数据传输

- 串音 (X-Talk) 与数据传输速度正相关

new version



old version

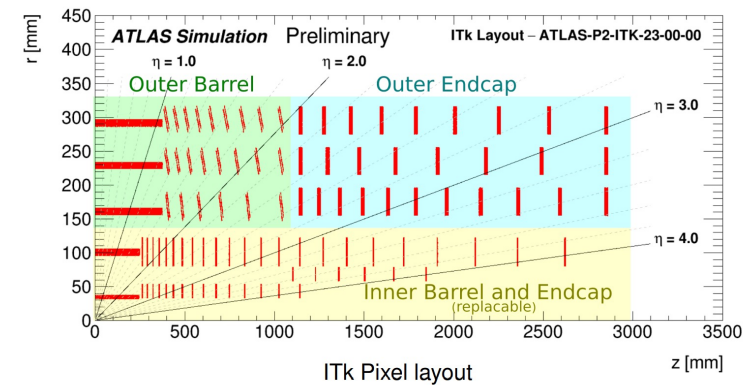
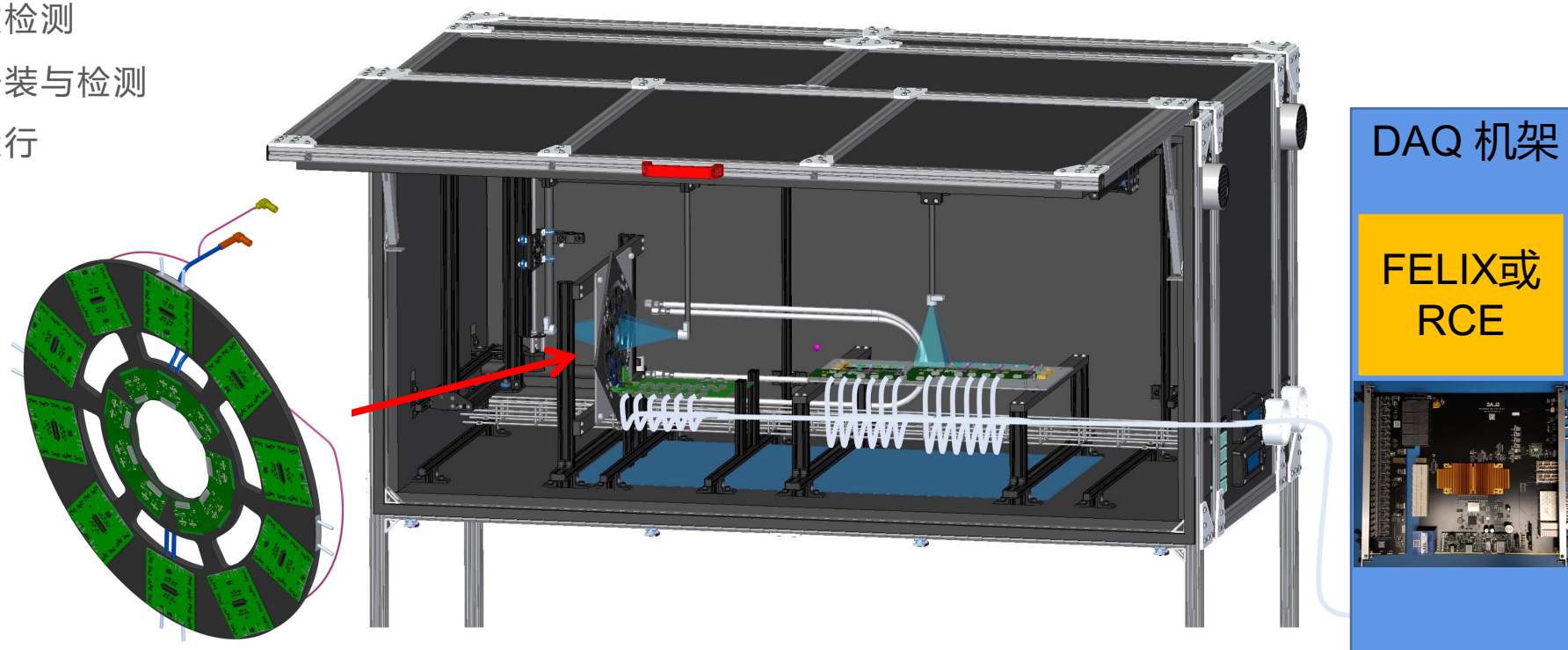


基于Rd53a的系统级展示样机

- 搭建系统级展示样机，用于验证组装流程、机械结构、热学、数据传输电路和读出系统等

- **电子学部分：**

- 探测器模块的接收检测
- 数据传输电路的安装与检测
- 读出系统开发与运行



Rd53a的系统级读出

Link Agg. Testing at SLAC Without FELIX

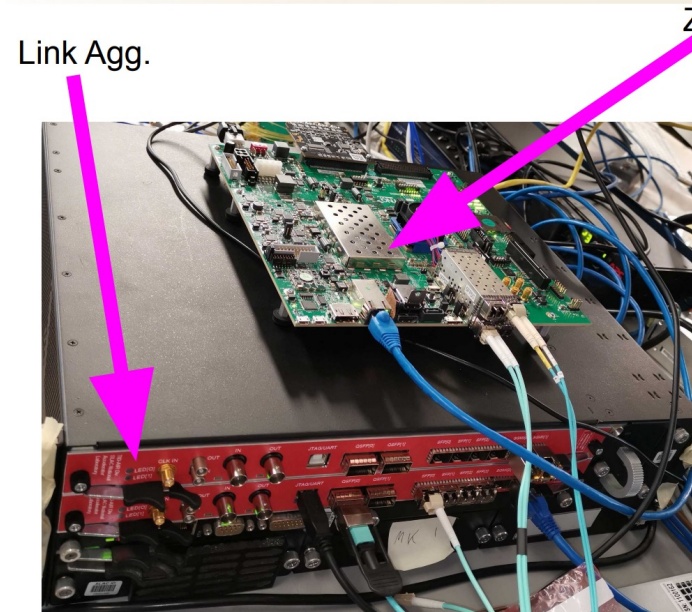


Revision C01 tested

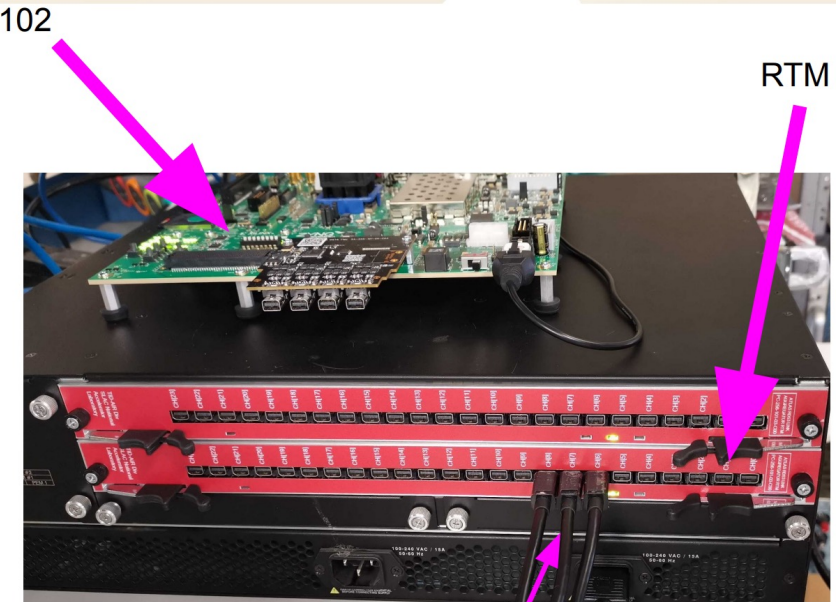
- no issue found
- 3 boards available
- (One C00 board at Gottingen, for joint IpGBT emulator development)

Communication between Aggregator FPGA and backend DAQ

- 2 QSFP, up to **16.3 Gb/s** (GTY)
- 4 SFP, up to **16.3 Gb/s** (GTH)
- Additional 2 SFP for 1GbE only (SGMII)
 - Sideband configuration/monitoring
 - Non-data path, slow controls only

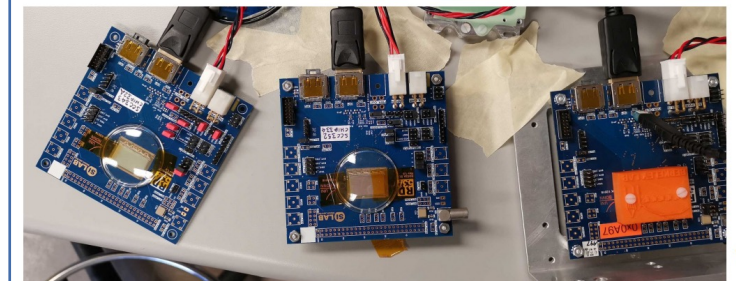


Front View



Rear View

Bonn RD53A SCC



- ZCU102 can readout **Rd53a at full speed** through FMC interface or SPF+ to IpGBT system
 - Retiming and Equalizer are essential
- ZCU102 + linkAgg succeeded in running chip calibration with 3 Rd53a SCC in parallel
 - 3 SCC in total at SLAC, more is better

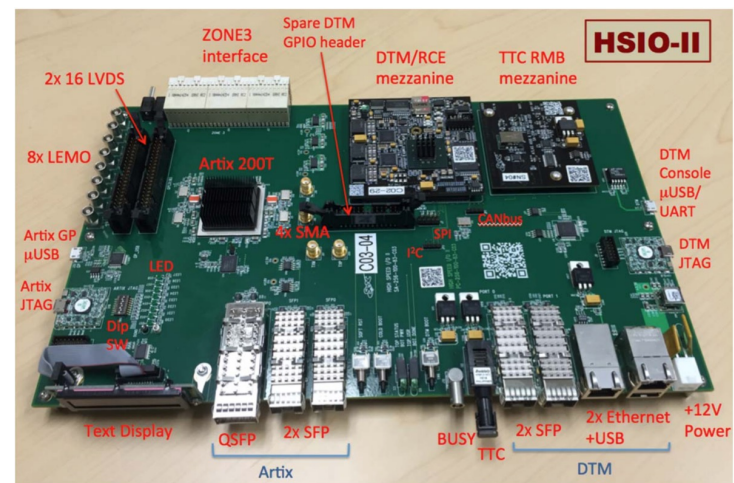
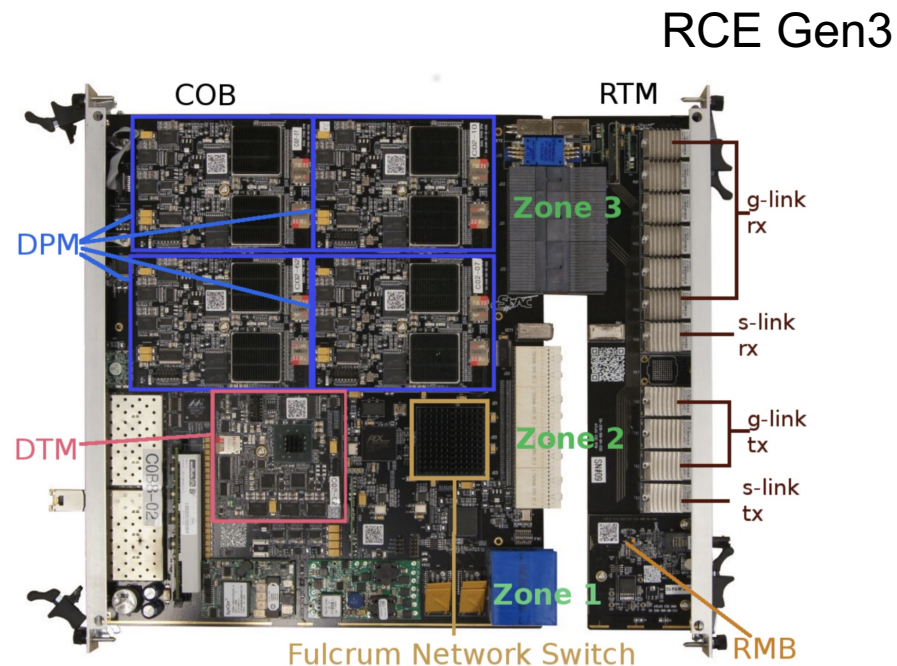
SLAC RCE SoC 平台

- 通用型SoC系统，适用于触发和读出，始于2007年

- 全称 Reconfigurable Cluster Element
- Xilinx Zynq芯片：集成了ARM CPU与FPGA
- 软件和固件协调开发
- 功能丰富：全覆盖高速与低速I/O端口

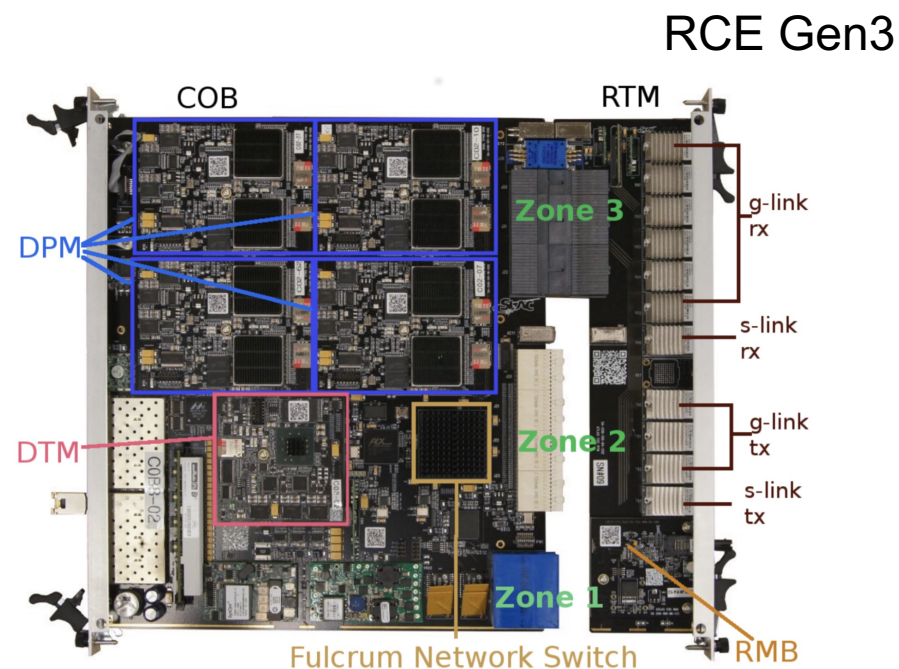
- Gen 3 (2013), based on **Zynq-7000** SoC

- 两套系统覆盖不同应用场景：COB（ATCA平台）和HSIO2
- COB（ATCA）：可靠，性能强，适用于大型数据处理
- HSIO2：与COB共用核心模块和设计，适用于小尺度（如探测器模块）快速部署和开发



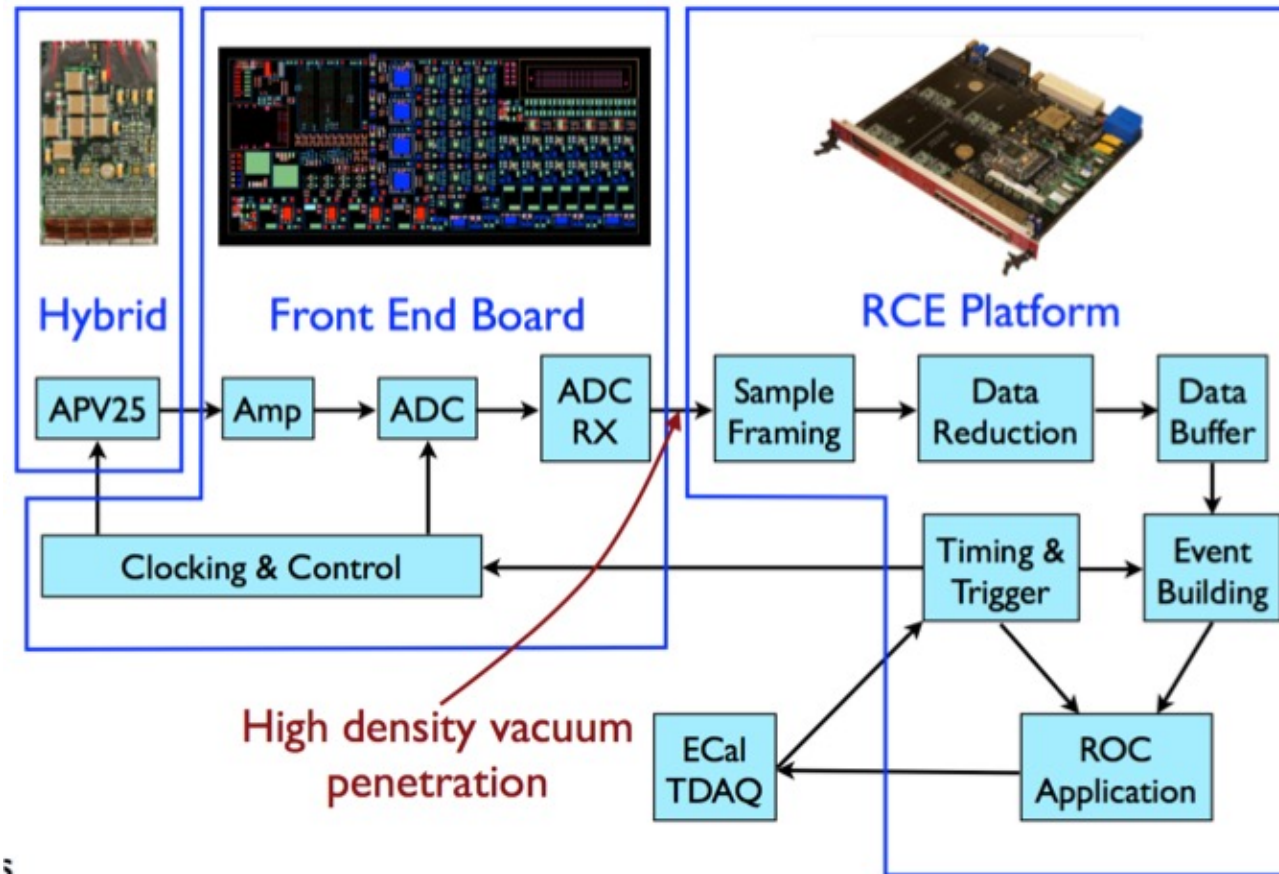
SLAC RCE SoC 平台

- ATLAS实验多处部署
 - CSC缪子读出系统（也是ATLAS实验里最早部署的基于ATCA平台的系统，2014）
 - ATLAS Run2 硅像素探测器IBL建造过程中的质量控制 Q/C
- 广泛用于各种其他物理实验，如巡天、暗物质、中微子、加速器控制等：LSST, HPS, protoDUNE, LCLS



RCE 用于SLAC重光子寻找实验HPS

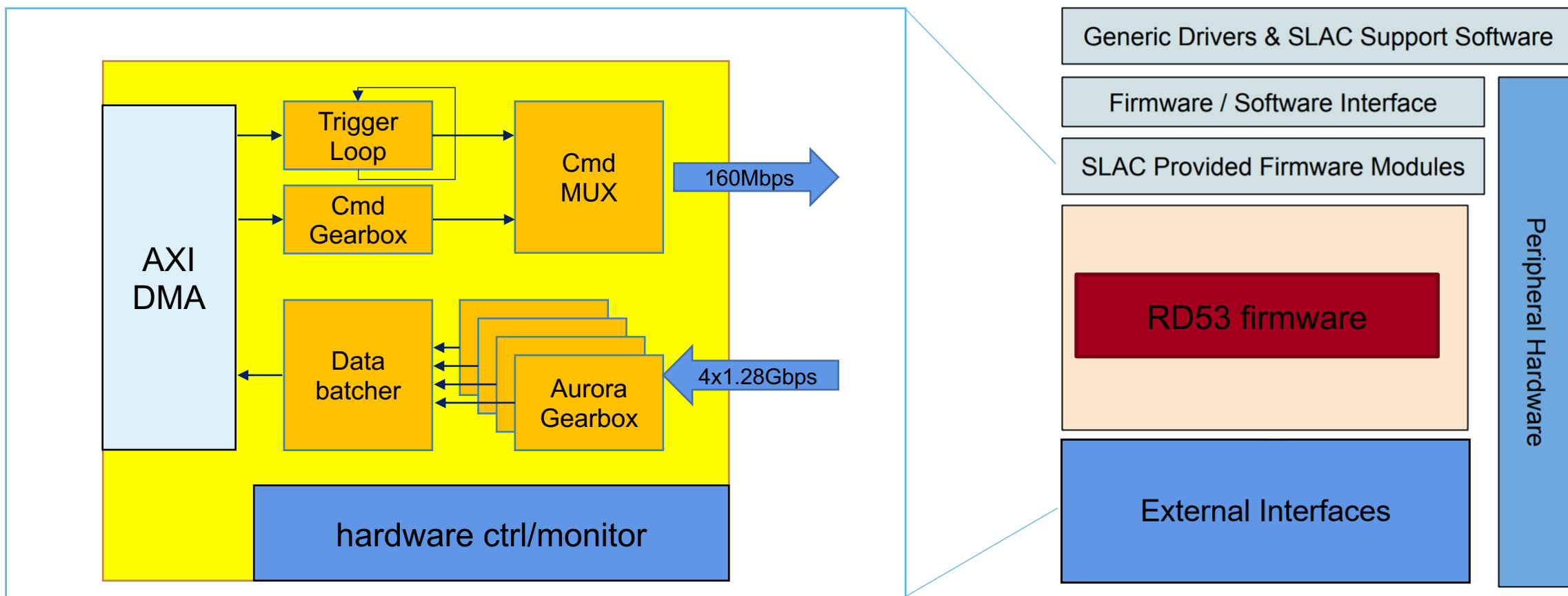
- The HPS Tracker Readout Electronics: continuous readout the SVT silicon detector modules



5

开源软件和固件协调开发

- <https://github.com/slaclab/atlas-rd53-fmc-dev>
- <https://github.com/slaclab/atlas-rd53-fw-lib>



Rd53a芯片的DAQ性能对比

- RCE Gen3 (2013)

- would be useful for the Rd53a based demonstrator operation in early 2022



*2021 summer intern, E. Kowalczyk, MSU

- comparing with other DAQs at same scan condition

- *YARR DAQ can only run Rd53a at half speed, 640Mbps

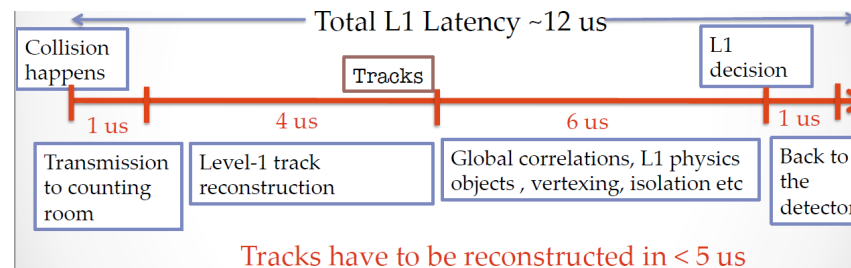
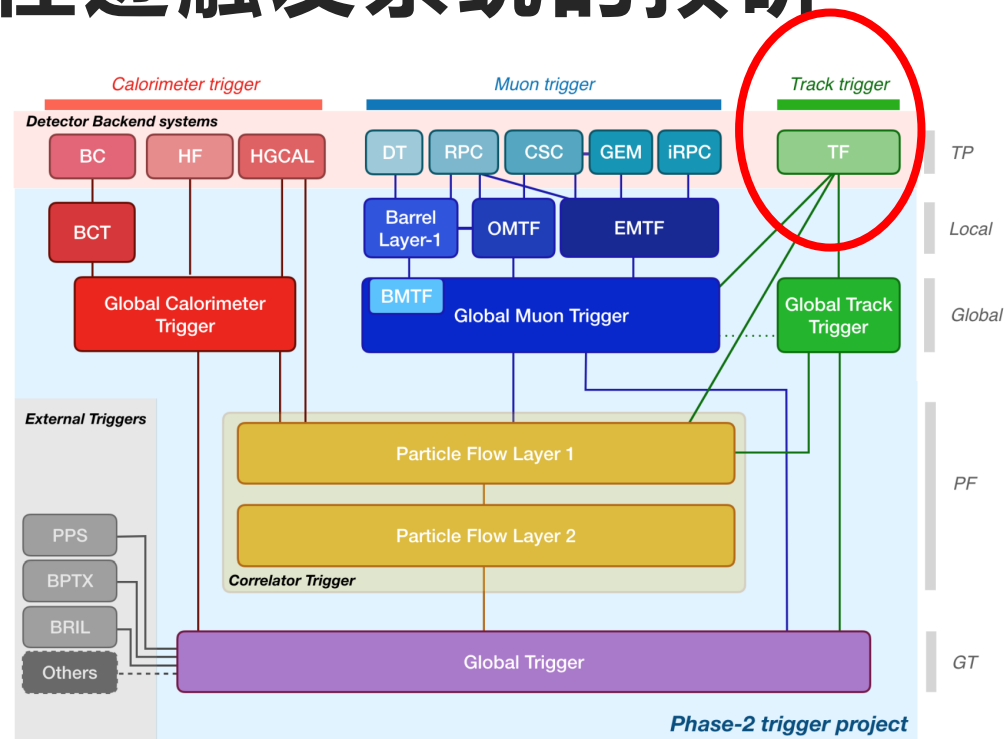
	YARR	RCE/ZCU102@640	RCE/ZCU102@1280	FELIX
digital scan	3.5 sec	1.3 sec	1.0 sec	20 sec
analog/TOT scan	3.5 sec	1.6 sec	-	-
threshold scan	100 sec	20 sec	-	-

CMS二期 Level-1 (硬件级) 径迹触发系统的预研

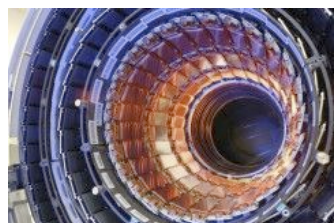
- 基于外层半导体径迹探测器 (Outer Tracker)

- CMS上无先例
- 海量原始数据 : 100 Tb/s
- 4 μ s内完成径迹重建

- 需在2017年初前完成展示样机



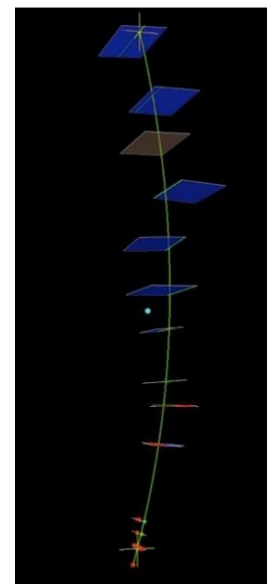
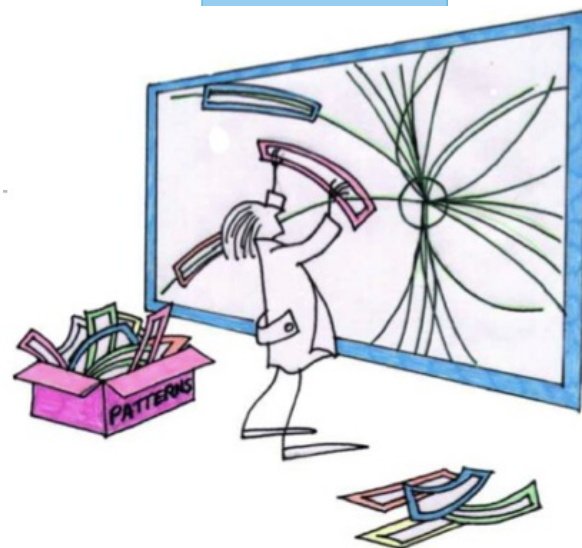
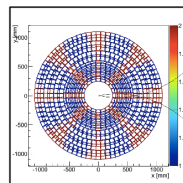
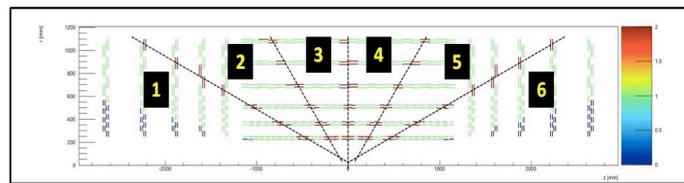
基于AM方法的径迹触发系统



数据传输

模式识别

径迹拟合



- 探测器分割为多个区域
- 每个区域由一台ATCA机箱负责接收数据

ATCA（先进电信计算平台）

- 工业标准，满足现代高速数据传输的需求
- 优异的散热和可靠性
- 电信、航天、工业控制、智能交通等
- CMS Phase 2: 从 μ TCA 迁移到ATCA平台

Associate Memory方法

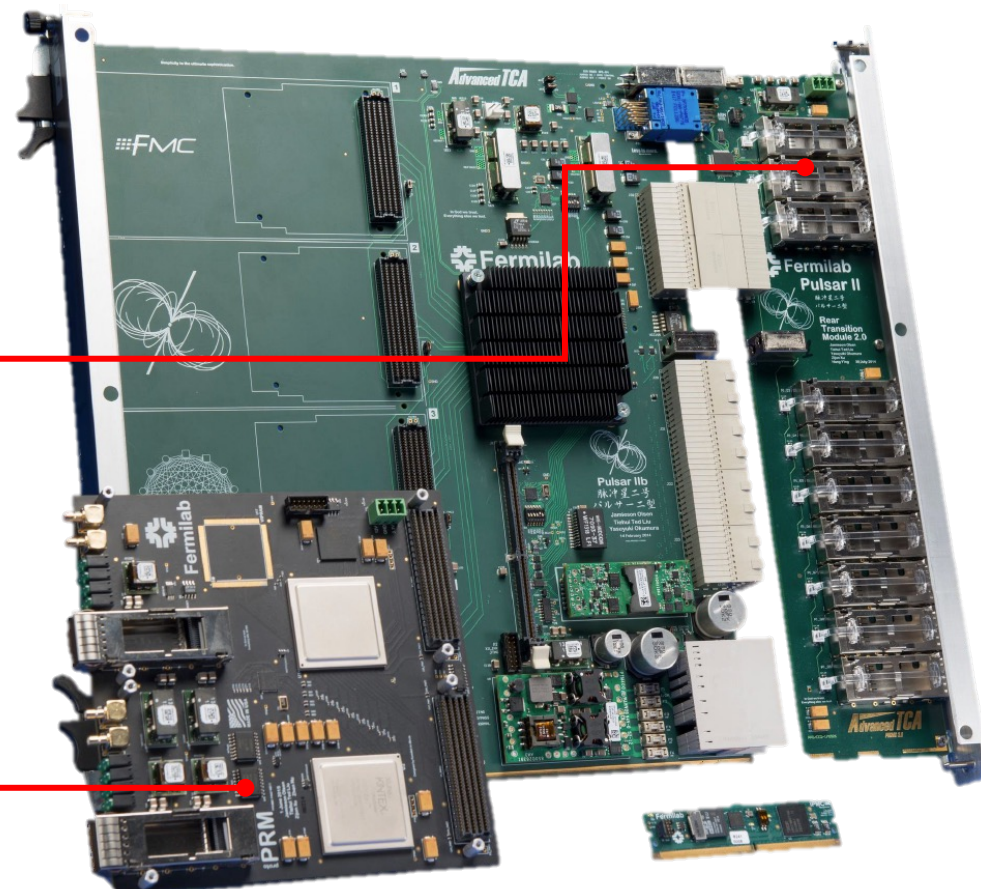
- 在Fermilab的CDF探测器上应用
- 提前计算所有可能的径迹模式
- 实时对比预存的径迹模式，快速识别所有可能
- 自研AM存储芯片：**高风险**

FPGA固件

- 线性算法快速拟合
- 低延迟

电路板全家福

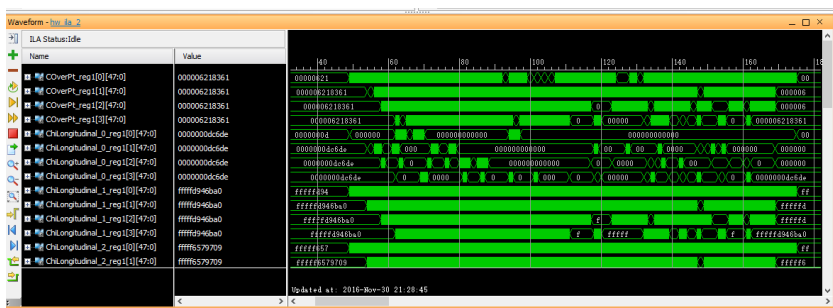
- ATCA计算平台
 - 先进的电信工业标准
 - 特点：性能强悍，设计灵活，可拓展，优异的散热和可靠性
- Pulsar2b 母板和背部传输模块（RTM）：
 - 符合ATCA标准
 - RTM接收探测器原始数据
 - 10个QSFP+插口，总输入带宽可达 $4 \times 10 \times 10 = 400$ Gb/s
 - 原始数据分发到夹板做径迹重建
- 双FPGA夹板，实现AM方法
 - 主FPGA用于接收原始数据和驱动AM芯片
 - 在AM芯片流片成功之前，使用从FPGA模拟AM芯片，用于系统展示和算法测试



*Pulsar2b电路板也用于 ATLAS Fast TracKer (FTK) 触发系统 ³¹

系统级展示样机

- 主导系统级展示样机的搭建和测试
 - 下机箱模拟探测器输出，上机箱演示触发系统
 - 480路光纤总带宽：4.8Tb/s
 - 背板总带宽：2.6Tb/s
 - 固件算法汇总在FPGA上运行
 - AM算法，北大；线性拟合，Texas A&M



- 径迹重建仅需 $2.5\mu\text{s}$ （满足 $<4\mu\text{s}$ 的要求）
- 结果进入[CMS二期Tracker TDR](#)，投稿NIMA

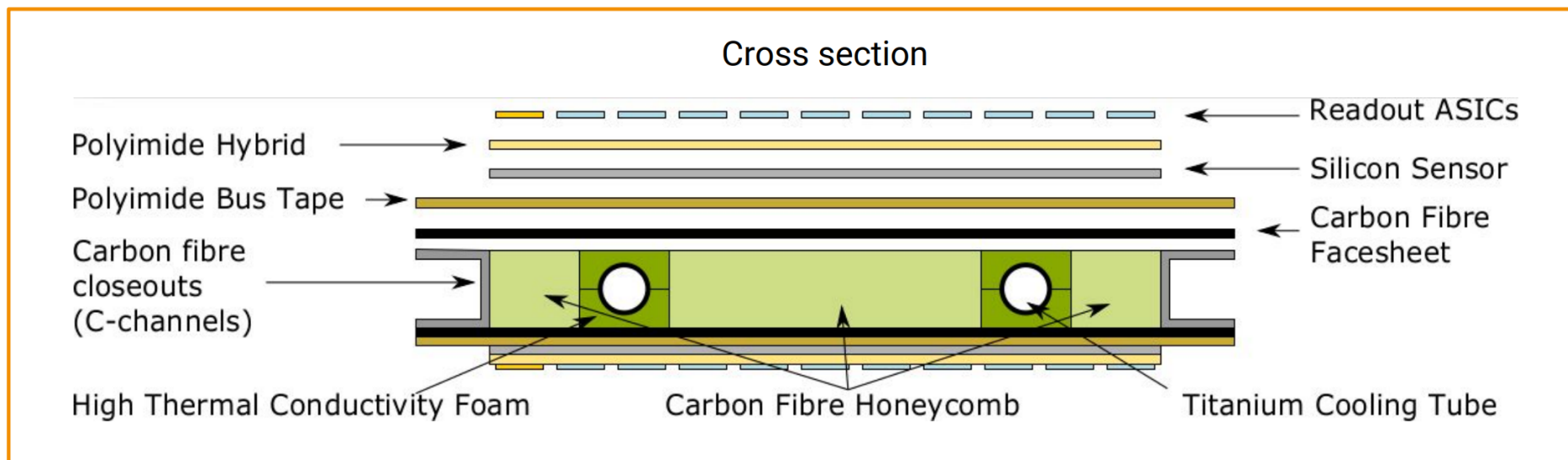
Back



感谢各位老师同学

System unit: a sandwich

- Modules directly glued on both sides of a light carbon-fiber support structure
- Cooling system embedded (bi-phase CO₂ cooling at -35°C)



👍 Minimizing material

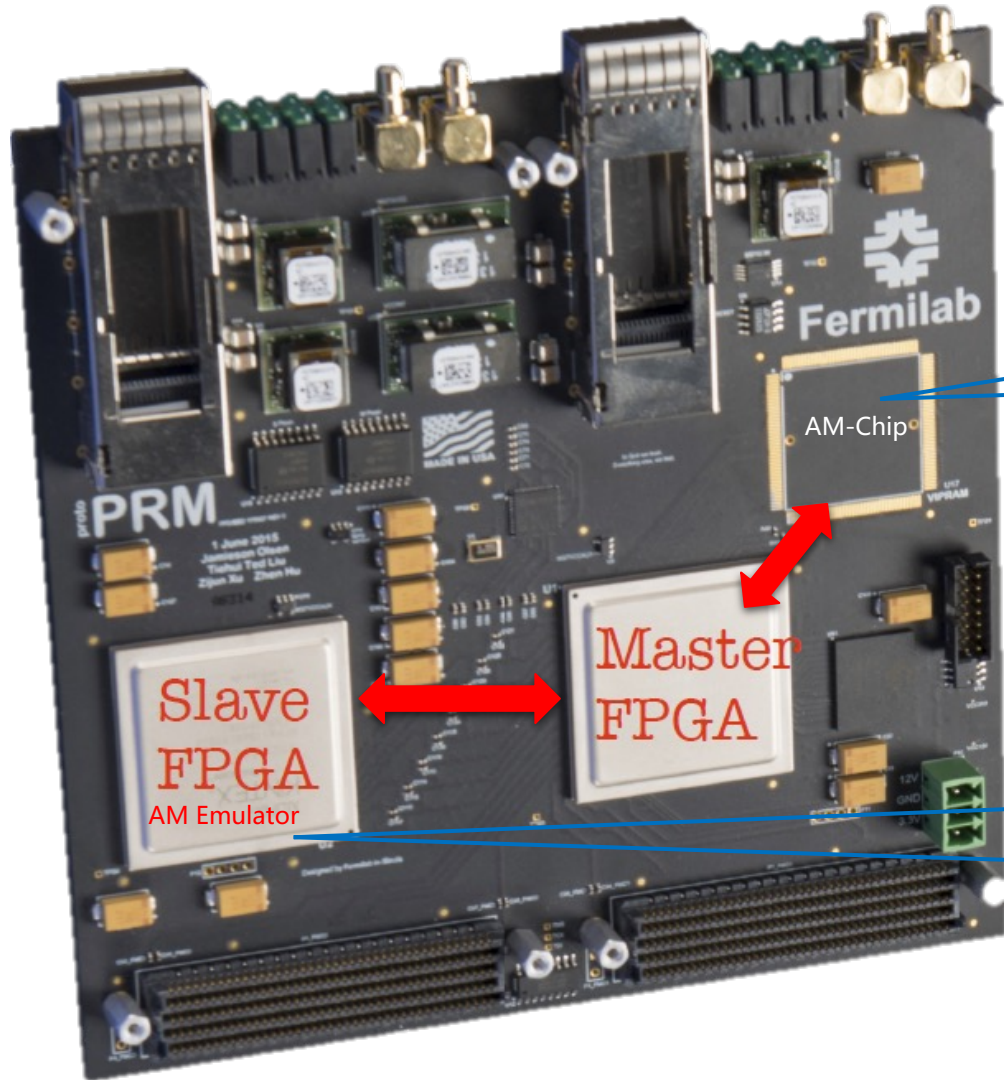
⇒ short thermal paths ~ 3 mm

⇒ reduced radiation length ~ 2% [x/X_0]

👍 Simplicity for large scale reproducibility

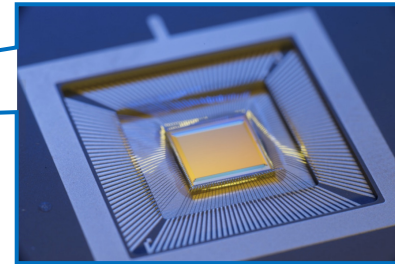
👍 Core and electronic components individually testable before assembly

AM ASIC and AM in FPGA



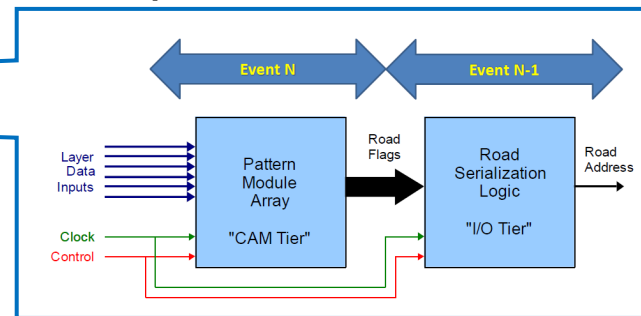
VIPRAM ASIC

- Vertically Integrated Pattern Recognition Associative Memory



AM Emulator

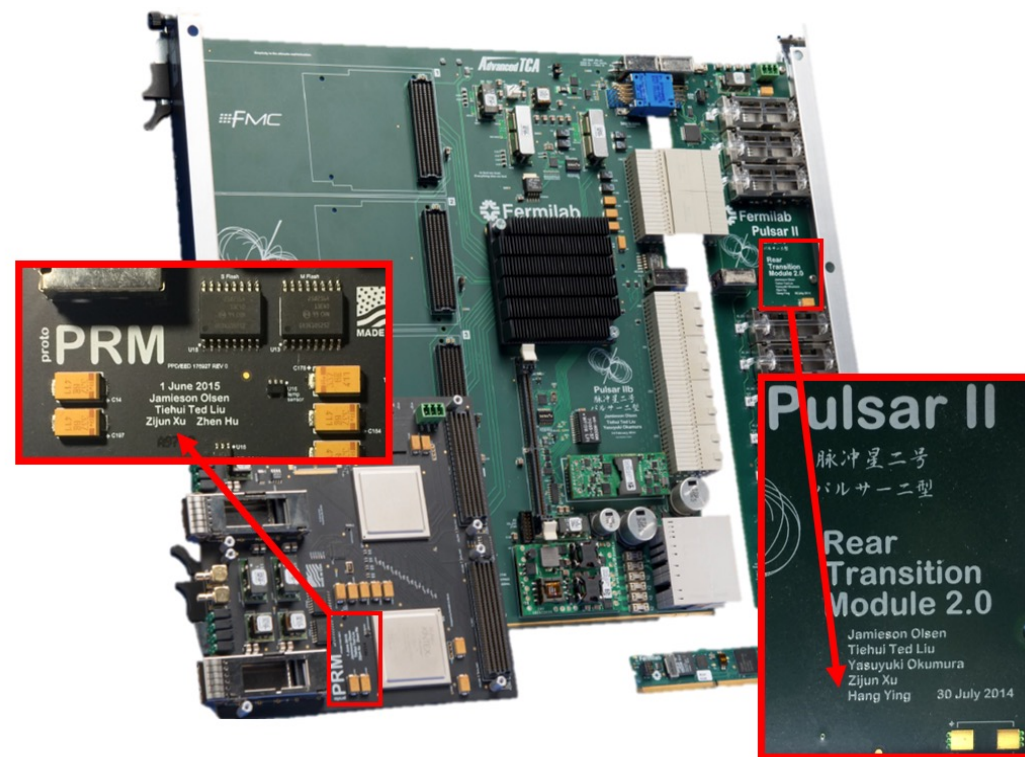
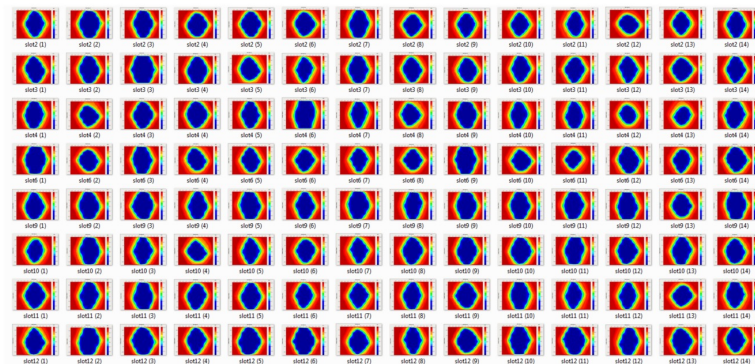
- FPGA implementation of VIPRAM ASIC



ATCA电路设计与FPGA固件开发


- 深度参与ATCA电路板设计，并负责测试
 - ATCA背板实测结果成为ATCA机箱厂家的展示样例
 - 电路设计和测试结果在IEEE NSS&MIC 做会议报告 [1]
- FPGA模拟AM芯片功能，用于算法研究和系统展示
 - 自研AM芯片生产延期
 - 针对FPGA硬件资源，提出新的模拟算法，保持AM核心功能
 - 内存容量从8k提高到了128k，接近芯片设计容量
 - 21st IEEE RTC报告 [2] 主要作者之一

8 Boards Installed in the Air-/Plane Shelf @ 10Gbps



1. "Pulsar IIb Design, System Integration and Next-Generation Full Mesh ATCA Backplane Test Results", IEEE NSS&MIC, 2015
2. "Implementation of a High-Performance Pattern Recognition Associative Memory in an FPGA", IEEE real time conference, 2018

DAQ data transmission performance for Rd53a

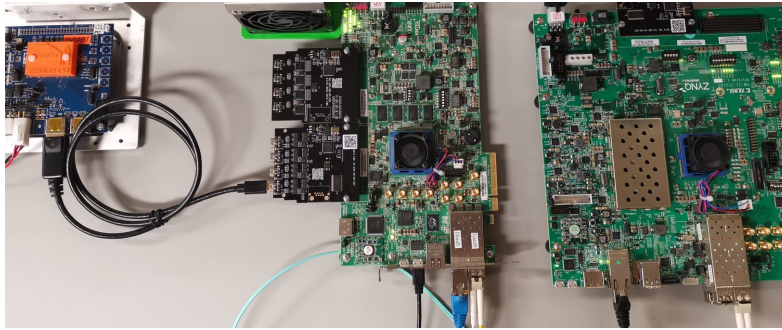
DAQ	Rd53a speed		electrical service max signal loss (-dB)	built-in Bit-Error-Rate Measurement
	640Mb/s	1.28Gb/s		
YARR	Yes	-	~10	-
direct FELIX	-	Yes	~10	xilinx IBERT tool, 2D eye-diagram
Optoboard + back-end DAQ	-	Yes	14	1D BER bathtub, step 50/100ps
RCE	Yes	Yes	17 	1D BER bathtub, step 3.5ps

- Rd53a has poor performance for data transmission, but it's the only available FE for demonstrator
- Optoboard/optobox is constraint by the availability of CERN IpGBT chip
- RCE can drive the Rd53a pixel demo system at full speed, 1.28Gb/s
 - full based on commercial ICs, the **data transmission feature(FMC adaptor) can easily scale up to ATCA** format to support large scale detector, O(100) FEs
 - full speed is crucial for testing the on-detector electrical service and stress test for FELIX DAQ

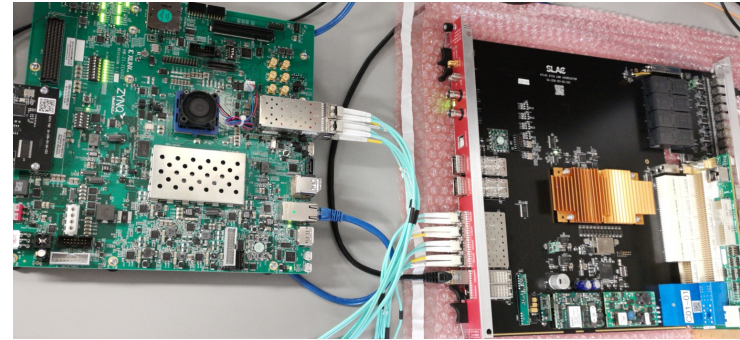
IpGBT + DAQ (FELIX或RCE)

- 在SLAC , 我搭建了Rd53 + IpGBT模拟系统 (linkAgg) + RCE DAQ系统用于测试新的硬件和固件

FMC+FPGA



ATCA



- 通过RCE DAQ获得的经验 , 帮助Argonne的同事开发FELIX DAQ (RCE的开发进度远领先于FELIX)

